Precision Physical Synthesis Users Manual

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About This Manual

Precision Physical Synthesis is a comprehensive tool suite, providing design capture in the form of VHDL and Verilog entry, advanced register- transfer-level logic synthesis, constraint-based optimization, state-of-the-art timing analysis, schematic viewing, encapsulated place-and-route, advanced physical synthesis algorithms and a physical editor. This manual describes the automated physical synthesis flow using the Precision Physical Synthesis Graphical User Interface (GUI) and provides information on how to use PreciseView to manually edit the physical placement.

For the Latest Information

From the time this document is published to the present, new information may have become available. Please refer to the web-based documents at the following address for the most current information. http://www.mentor.com/precision/download

Chapter 1
Introduction

Introduction to Physical Synthesis

Precision Physical Synthesis is a product that extends the features of Precision RTL Synthesis by adding an Automated Physical Synthesis Flow and an Interactive Fix-up Environment. Precision Physical Synthesis can also be used to achieve timing closure on designs that have been synthesized by another third party synthesis tool.

Physical Synthesis is the process of combining physical information (Place & Route data) with synthesis algorithms to produce better performance and overall quality of results (QofR). The physical synthesis features are made active after you run your design through Precision RTL synthesis and run a first pass Place & Route with the vendor implementation tools. Currently Virtex-E and Virtex-II are supported. The physical synthesis algorithms perform three optimization techniques: (1) re-timing, (2) replication, and (3) re-synthesis.

Re-timing balances the positive and negative slacks found throughout the implemented design. Once the node slacks are calculated, registers are moved across logic to borrow positive slack time to improve critical timing. Re-timing is commonly done during RTL synthesis, however, the wire load models that are used are only estimates the interconnect delay. During physical synthesis, re-timing is done with the actual interconnect delays which is far more accurate. This is important because interconnect delay in a large FPGA design is a dominant factor in total delay.

Replication is a technique that is especially effective in breaking up long interconnects at the physical level. During RTL synthesis, replication is performed at the logic level based on wire-load models to honor fanout restrictions. The physical optimization flow builds on the RTL synthesis results by using more accurate data from the physical layout. In addition, the replication algorithms understand what resources are available in the target device and makes intelligent choices as to what logic or registers to replicate and where to place these replicated registers.

Re-synthesis is a technique that uses the physical data to make local optimizations to critical paths. Re-synthesis uses operations like logic restructuring, re-clustering, substitution and/or possible elimination of gates and wires to improve timing and routability. Precision Physical

Synthesis works with incremental placement to understand what resources are available in the target device and how the changes impact routing congestion and delays.

Setting Up the Environment

Installation

Refer to the Precision Synthesis Installation Manual for details about installing Precision Physical Synthesis.

Setting Xilinx Environment Variables

PAR_BELDLYRPT = 1

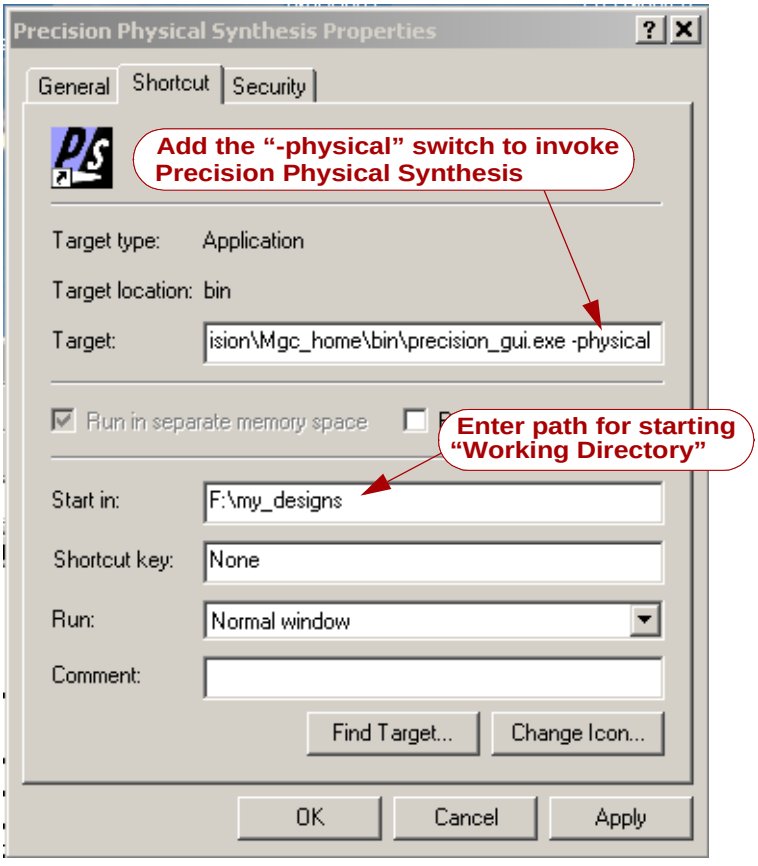
Precision Physical Synthesis requires that Xilinx ISE tools generate a DLY file that contains the interconnect delays from Place and Route. You must set the environment variable PAR_BELDLYRPT to 1 (true) in order to make sure that the DLY file is generated.

Invoking the Tool

Invoking the Precision Physical Synthesis GUI

You invoke the Precision Physical Synthesis GUI by entering the `precision` command with the **-physical** option from a Windows shell or a Unix shell. Use the **-physical_sa** option to invoke Precision Physical-SA (Stand-Alone) GUI. When you install the product in a Windows environment, three Shortcut icons are placed on the Desktop. One for Precision RTL Synthesis, one for Precision Physical, and one for Precision Physical-SA. The difference between each icon is the command option specified at the end of the invocation line. As shown in Figure 1-1, the **-physical** option is added to the executable call for Precision Physical Synthesis. If you replace the **-physical** option switch with **-rtl**, only the RTL Synthesis features are invoked. Similarly, the **-physical_sa** option invokes Precision with only Precision Physical functionality. All RTL Synthesis features will be unavailable.

Figure 1-1. Setting Up the Precision RTL Synthesis Shortcut



Invoking Precision Physical Synthesis from a Shell

You can invoke Precision Physical and Physical-SA in non-GUI mode by using the following commands respectively:

```
precision -shell -physical
precision -shell -physical_sa
```

In non-GUI mode you can source Tcl scripts or you can interactively enter commands from the shell prompt. A typical command line entry might be the following where a Tcl command file is specified to set constraints and guide the tool through the synthesis process:

```
% precision -shell -physical -file dofile.tcl
```

The `precision` command and its optional switches is fully documented in the section titled Commands in the Precision Synthesis Reference Manual.

Note

When you invoke the tool in non-GUI mode, the -shell option should be specified first in the options list (as shown above).

Chapter 2
The Integrated Physical Synthesis Flow

The Integrated Physical Synthesis flow assumes that you are using Precision Physical Synthesis to synthesize your HDL design and that you invoke the Xilinx ISE tools from the Precision GUI. The steps in the flow are as follows:

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Step 1: Setting Up a Project

Precision Physical includes the Project Manager to help you manage the data created during the iterative synthesis process. The Project Manager offers a framework that supports and promotes a design process based on experimentation. The Project Manager system is based on *projects* which contain multiple *implementations*. Each implementation within a project is a separate workspace in which you can experiment with different synthesis strategies and configurations. Implementations keep track of all of the design settings, input files, and output files that comprise its configuration. The Project Manager facilitates your design efforts by allowing you to create, delete, copy, edit and save implementations.

After creating a project and its implementation(s), proceed with your synthesis design flow. Before closing the project, save the current state of the active implementation. Then the next time you open the project, it will be restored to the state it was in when you closed it.

The Project Manager is accessible in all user interface modes; Graphical User Interface (GUI), Tcl command line in the Transcript window or the shell window, and Tcl scripts when running Precision in batch mode. Precision provides Tcl commands that correspond to all of the Project Manager menus and Design Bar icons, as well as other supporting commands.

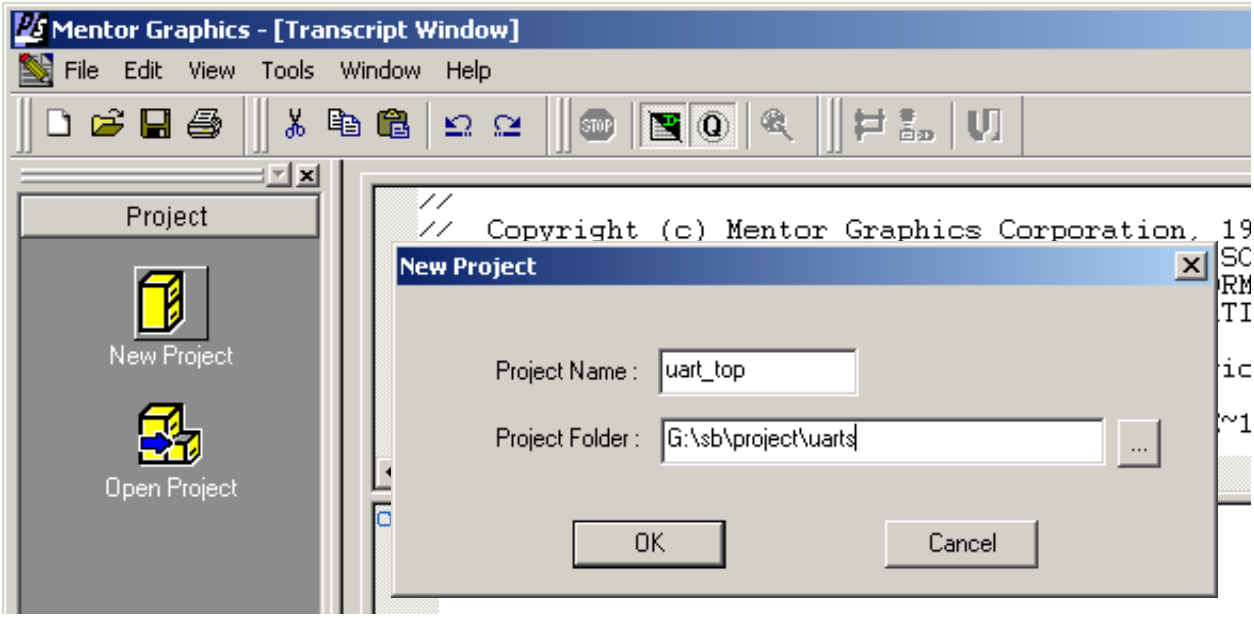
Creating a Project

The Project Manager is enabled by opening or creating a project. From that point until you close the project, all of your work is carried out in the context of the active implementation in that project.

When you invoke Precision Physical, the session window displays the Design Bar and the transcript window. The Design Bar displays the “Project” pane which is where all project related icons are found. Initially it contains only 2 icons: **New Project** and **Open Project**. More appear after a project is open.

To create a project either click on the **New Project** icon on the Design Bar, or choose the **File** > **New Project** menu. Precision opens the New Project dialog box, as shown in Figure 2-1.

Figure 2-1. Initial Session Window and New Project Dialog Box



When you OK the dialog box, the project and an initial *implementation* are created and opened in the Design Center window, as shown in the figure above. For detailed instructions on how to use the Project Manager, see “Chapter 4: Project Manager” in the *Precision RTL Synthesis Users Manual*.

Step 2: Synthesize Your Xilinx Design

Figure 2-2. Step 1: Synthesize Your Xilinx Design

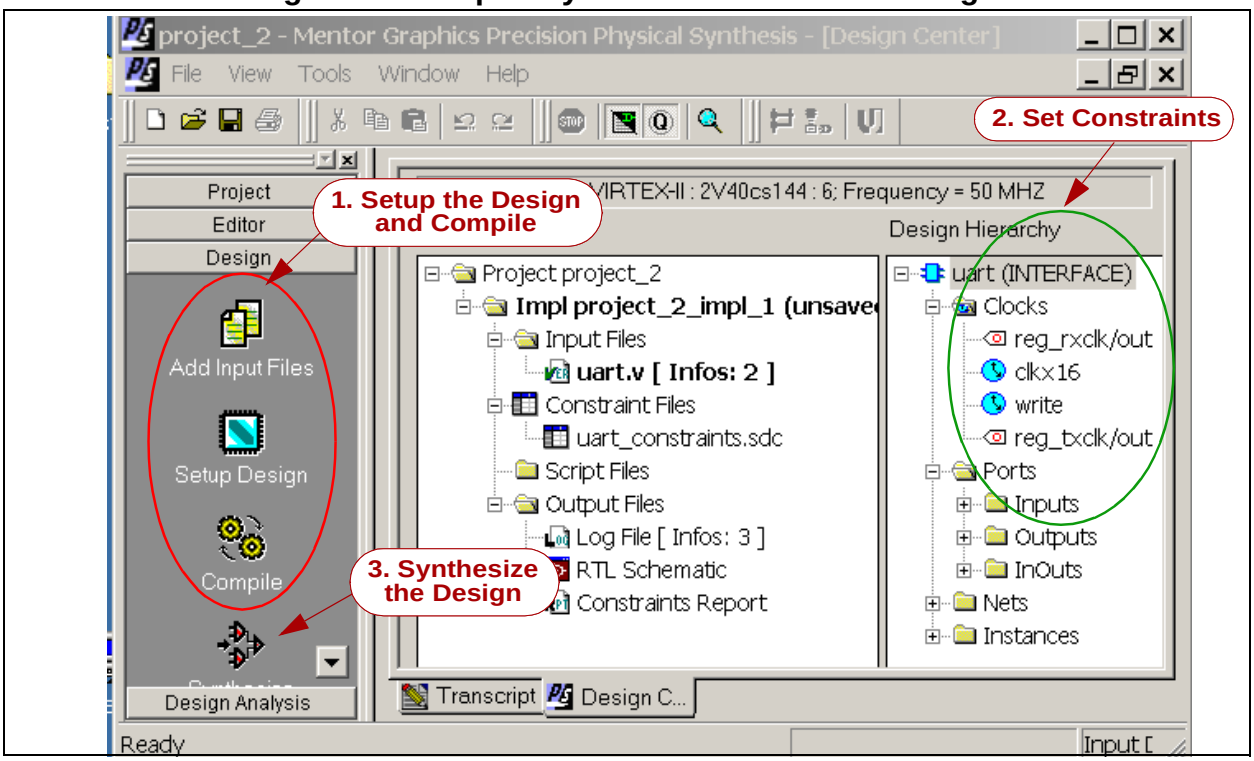
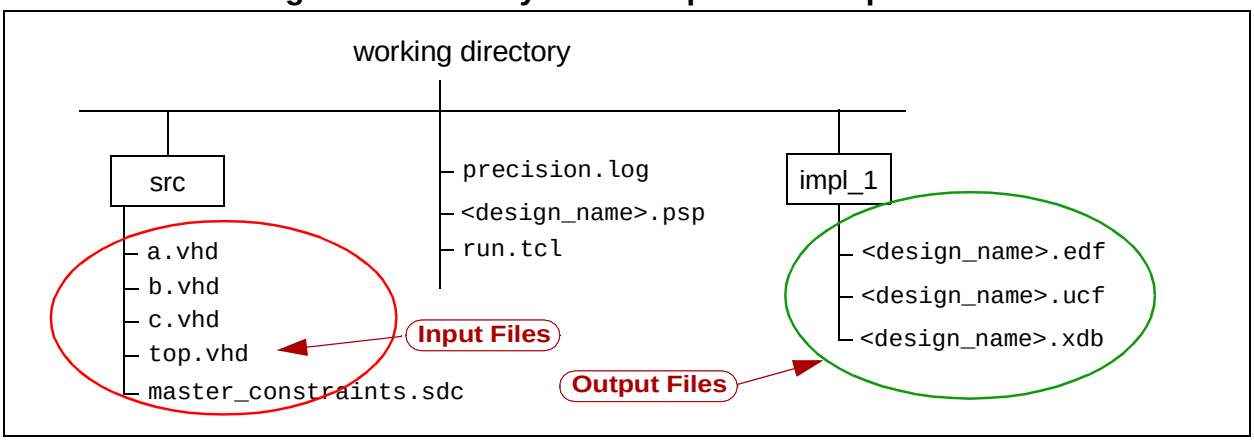


Figure 2-3. RTL Synthesis Input and Output Files



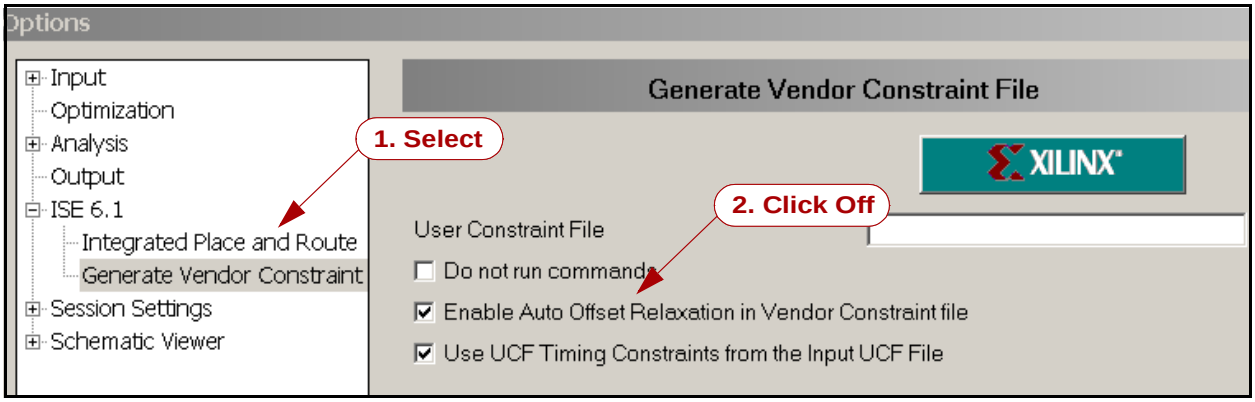
File Extension	RTL Synthesis Output File Description
.edf	Output Design in EDIF format.
.ucf	Generated constraint file for ISE (user constraint format)
.xdb	Output design in Mentor Graphics binary format.

The illustrations on the left show the general sequence of steps required to synthesize your design with Precision. Complete information on Compiling, Setting Constraints, and Synthesizing can be found in the Precision RTL Synthesis User's Manual starting on page 2-1. Information on how to setup a project using a Tcl script can be found on page 2-17.

Eliminating Relaxed Constraints

If the constraints you specify in RTL synthesis are too tight and impossible for Place and Route (PAR) to meet, the ISE tools will report an error and fail to finish. To prevent this from happening, Precision has an option that will automatically relax an impossible constraint and allow PAR to finish. The tradeoff is that a relaxed constraint may cause true critical paths to be ignored. It is important to turn off this Precision option if you are using physical synthesis. As shown below, after you select the Xilinx technology, use the pulldown menu **Tools > Set Options >ISE 6.1 > Generate Vendor Constraint File** dialog to disable the option.

Figure 2-4. Generate Vendor Constraints



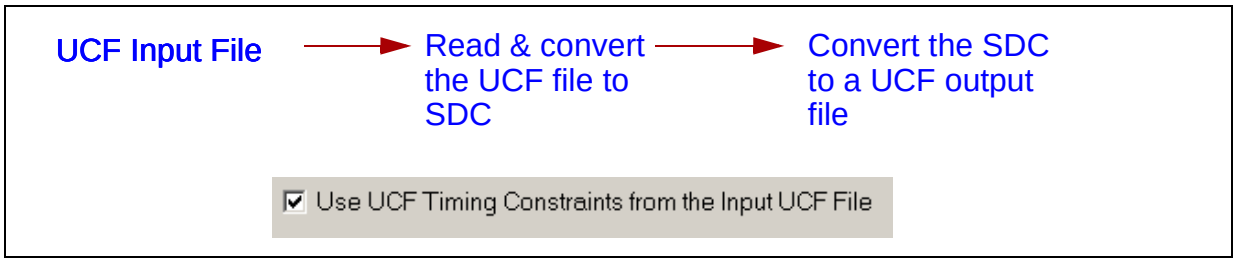
Use UCF Timing Constraints from the Input UCF File

Precision will automatically generate and manage your constraints files. The designer can read in existing SDC constraint files, which can be edited in the GUI, or all constraints can be produced in the GUI. In either case, an output SDC file is created and maintained by the tool. This allows you to use this standard file for other downstream tools. Additionally, when timing optimization is run, the timing report is generated and this file is managed along with other project data.

The Precision Physical tool also lets you use a UCF input file to determine timing constraints. You can select this option from the Generate Constraints File dialog shown in Figure 2-4. The

UCF options available in the tool are either use (default, with the box checked) or don't use of a UCF file. The following figure shows the effects of this selection.

Figure 2-5. Default UCF Options

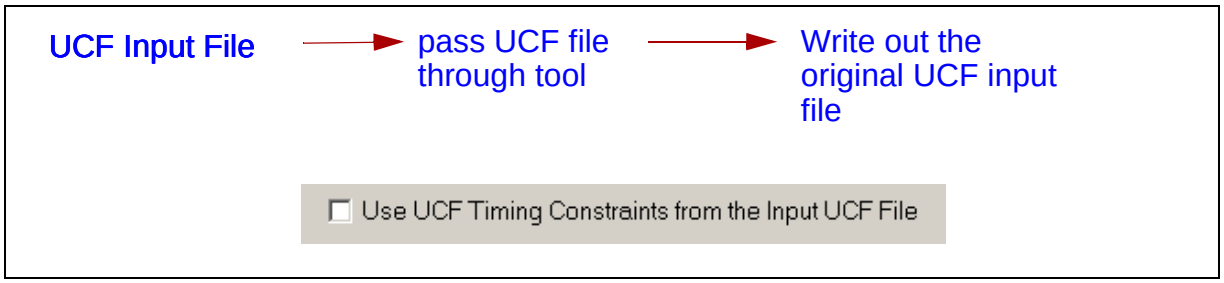

UCF Input File
Read & convert the UCF file to SDC
Convert the SDC to a UCF output file
Use UCF Timing Constraints from the Input UCF File

Use the UCF File without Conversion

There may be times when you want to use the UCF file without having the Precision Physical tool take any action on the file. An example of this is a design that contains a "black box" within a design. If you want the UCF file passed through the tool without conversion, deselect the checkbox in the "Use UCF Timing Constraints from the UCF Input File." The effects are shown in the following figure:

In this case, the file is read in and passes through the tool without being converted to SDC.

Figure 2-6. Pass-through UCF Options


UCF Input File
pass UCF file through tool
Write out the original UCF input file
Use UCF Timing Constraints from the Input UCF File

RTL Synthesis Output Files

The output files from Precision are placed in the current implementation directory. This directory will be used as the project directory for ISE. The files of interest to Place and Route are the EDF file and the UCF file. The EDF file is your synthesized design in EDIF format. The UCF (Xilinx user constraint format) file contains the constraints that you applied to the synthesized design.

An additional file of interest is the XDB file. This file is your design database in Precision binary format. It is equivalent to the content of both the EDF file and UCF file and will be used as a Precision input file in Step 3.

Step 3: Run First Pass Place & Route

Figure 2-7. Running Place and Route

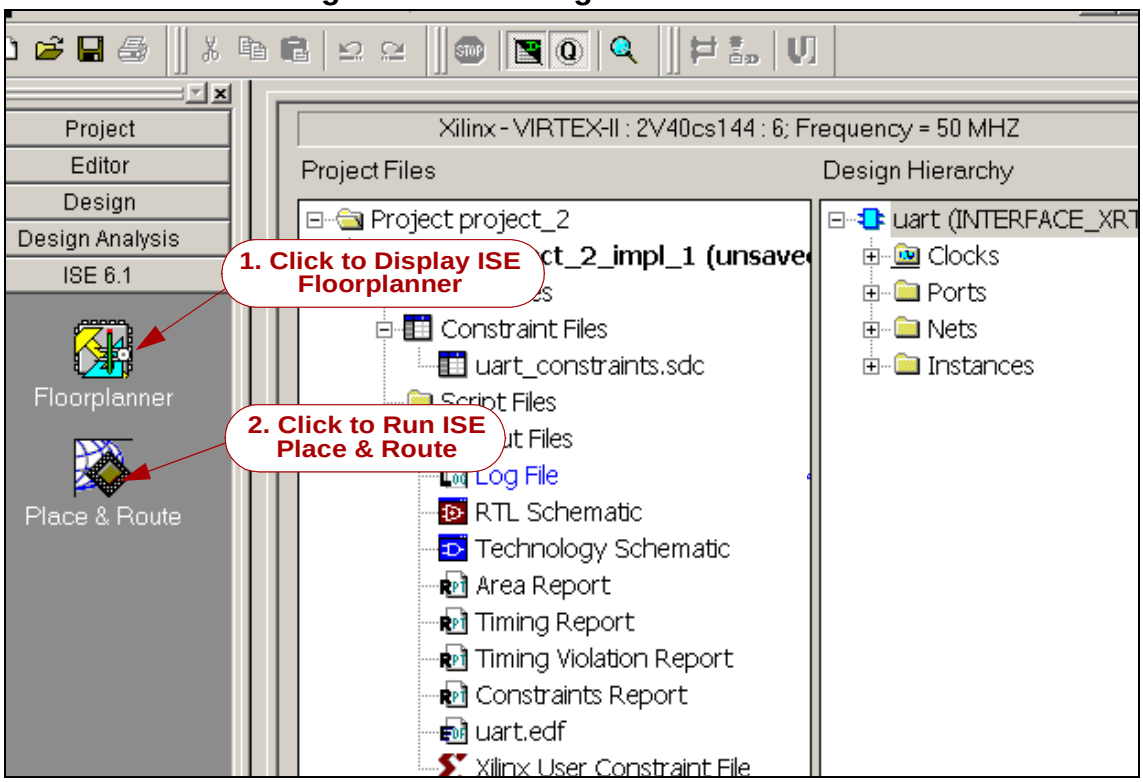
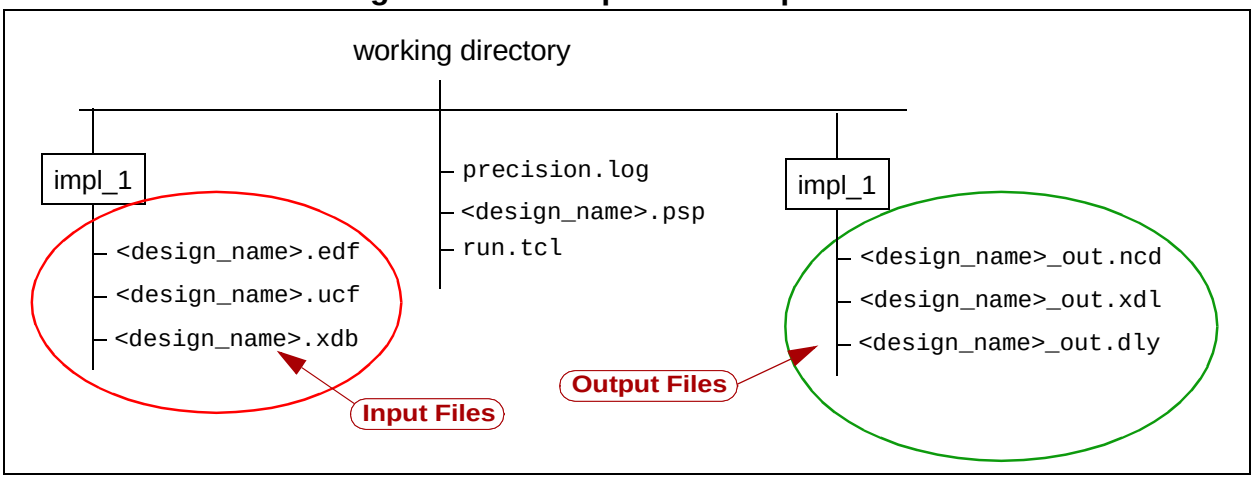


Figure 2-8. ISE Input and Output Files



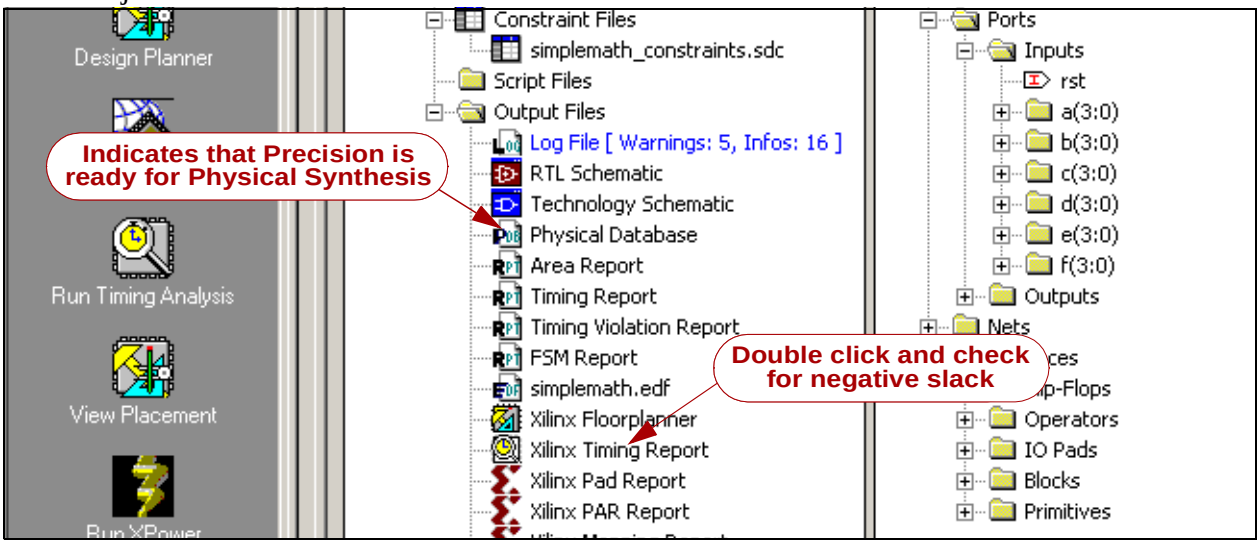
File Extension	Place & Route Output File Descriptions
*_out.ncd	Implemented design in Xilinx proprietary (binary) format
*_out.xdl	Implemented design in Xilinx xdl netlist format
*_out.dly	A file containing the true interconnect delays

The graphics on the left in Figure 2-7 show how you can invoke the Xilinx ISE tools from the Precision Physical GUI. ISE uses the EDF and the UCF file as input. Also, if you compiled the HDL design with a Xilinx UCF file in the Input File List, that file will be passed through to the implementation directory and will be picked up by ISE during the implementation.

When the implementation is complete, the NCD file and the DLY file are placed back in the implementation directory with the characters "**_out**" appended to the design name. The NCD file is your implemented design in Xilinx proprietary (binary) format. The DLY file contains the interconnect delays. The XDL file contains the placement data and is automatically created by Precision using the Xilinx *xdl* utility.

The Automatic Building of the Physical Database

Precision uses the input files XDB, XDL, and DLY to automatically create an in-memory physical database. When the creation process is finished, the Physical Database icon appears in the Project browser as shown below.



Checking the Xilinx Timing Report

It is common at this point to double-click on the Xilinx Timing Report and see if the implementation meets timing. If you find positive slack, you are finished. If you find negative slack, proceed to the Step 4.

Running Place & Route Separately

If you have a large design it may take several hours to run Place & Route and you may choose to run ISE separately from a shell. The output is a Xilinx NCD file and a DLY file. To create a Precision Physical database, you add this NCD file, the DLY file, and the original Precision-generated XDB file to the Input File List and Compile. You then click on the Physical Design Bar and run the automated Physical Synthesis algorithms or invoke PreciseView and proceed to improve the timing with Interactive Fix-Up.

Step 4: Run the Automated Physical Synthesis Flow

To run the Physical Synthesis Automated Flow, click on the **PreciseView** tool bar as shown below, then click on the **Physical Synthesis** icon.

Figure 2-9. Run Physical Synthesis

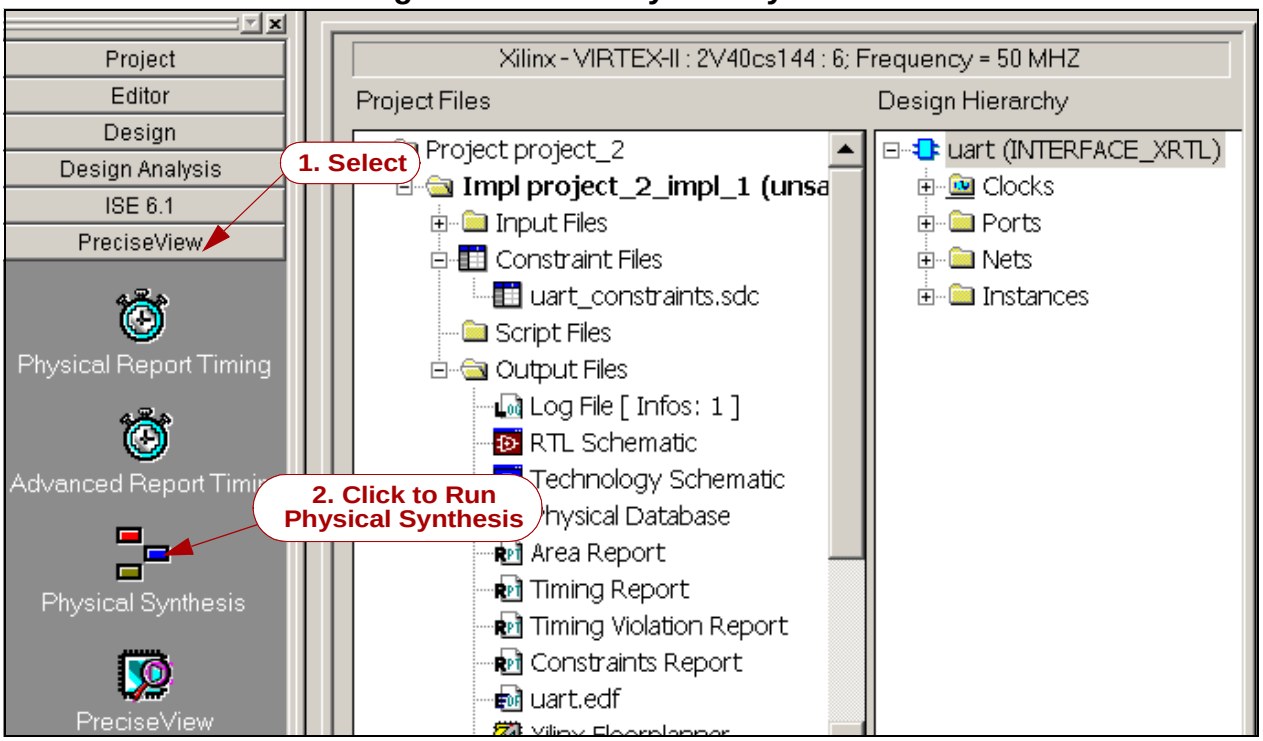
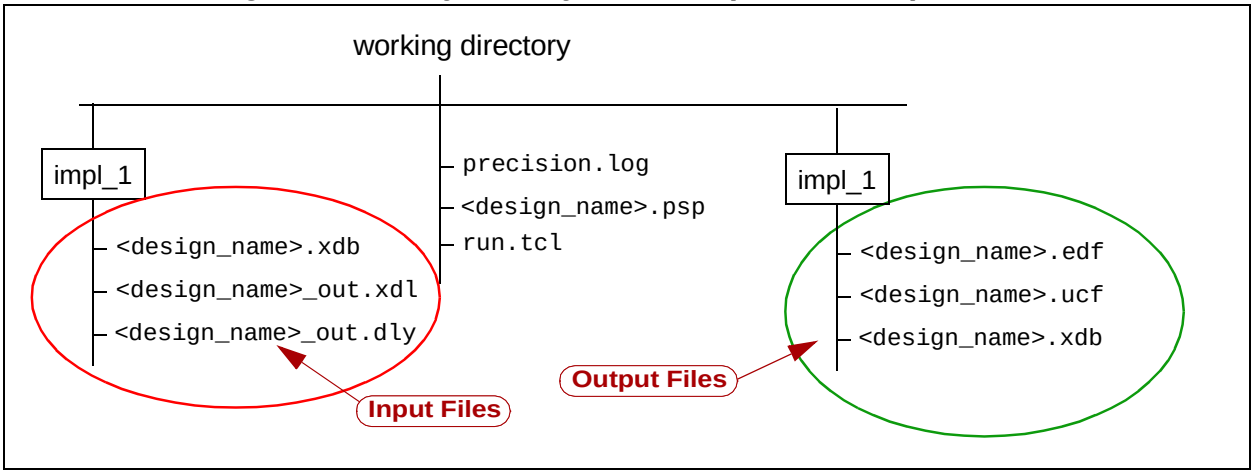


Figure 2-10. Physical Synthesis Input and Output Files



As shown in the graphics on the left in Figure 2-9, you click on the **PreciseView** tool bar, then click on the **Physical Synthesis** icon to invoke the automated physical synthesis flow. Precision runs the global physical synthesis algorithms on the whole design, generates a new timing report, and brings up the PreciseView editor with critical paths displayed. The results are then saved to the current implementation directory. The output files contain the original design data as well as the new physical placement information. New EDF, UCF, and XDB files overwrite the original output files by the same name. Other files of interest are the PDB file which is the PreciseView placement database and the FDB file which is the PreciseView floorplanning database. These files are saved so that you can restore the state the PreciseView editing session at a later time, if you wish.

At this point you should check the Physical Timing Report for positive slack on the most critical path. If you find positive slack, you are ready to run a 2nd pass Place & Route. If you find negative slack, you can proceed to use the PreciseView editor to locally optimization timing paths and/or manual move instances to improve the timing. The PreciseView timing engine is interactive so you can generate a new timing report at any time to check for improved timing.

Step 5: Re-run Place & Route and Check Timing

After you Save the results of any additional editing you may have done, you click the **Place & Route** icon on the ISE Design Bar and re-implement the design. Next, check the Xilinx Timing Report to see if the timing improved. You may repeat the Physical Synthesis flow as many times as you like to see if the timing can be improved. Or you can move to the Interactive Fix-Up Environment to see if you can manually improve the layout and routing on critical paths.

Note

If after physical synthesis you are running the second pass Place and Route with ISE outside of the Precision GUI, then you need to set the environment variable XIL_PAR_SKIPAUTOCLOCKPLACEMENT to 1. Otherwise, ISE may stop execution and complain of clock quadrant violations.

Chapter 3
PreciseView Basics

Effecting editing with PreciseView involves performing editing actions in combination with changing the display options so you can focus on various parts of the design layout. This Chapter describes the basics of executing the PreciseView features and changing the PreciseView display options.

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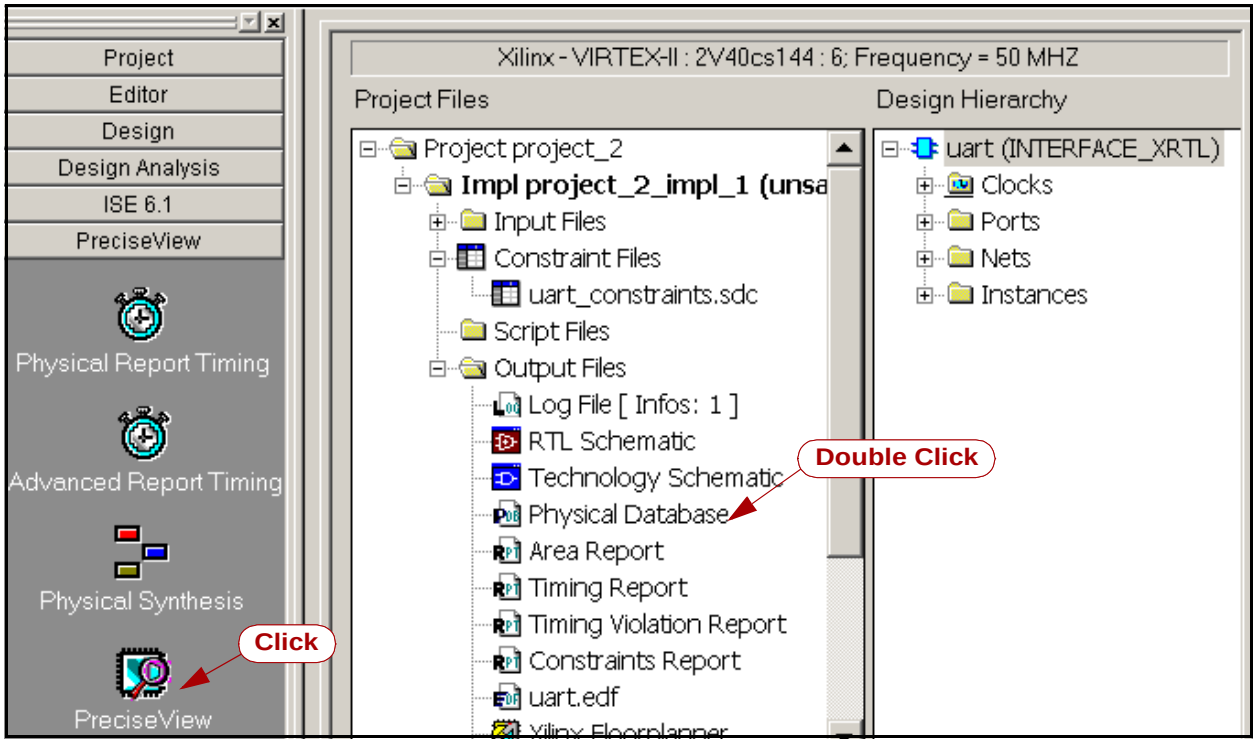
Invoking PreciseView

The PreciseView Editor allows you to do detailed editing of instance placement using a variety of functions. As shown below, you invoke PreciseView by clicking on the **PreciseView** icon in the PreciseView Bar or you can double-click on the **Physical Database** icon in the Project Browser.

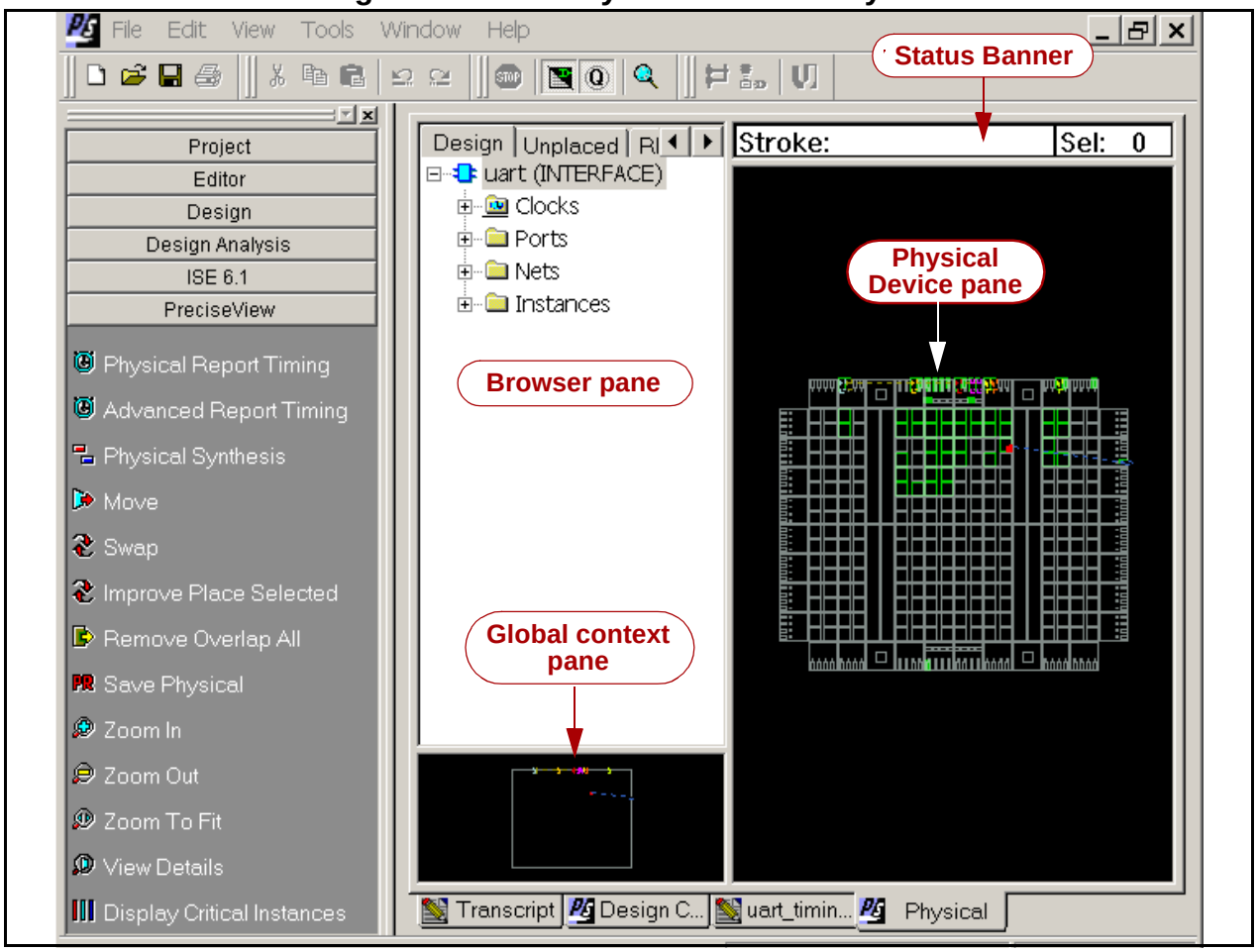
Figure 3-1. Invoking PreciseView



The Physical Window Layout

The Physical window is divided into three panes and a status banner. The Physical Device pane displays the physical layout of the chip and how the design instances are placed in the chip. The Browser pane allows you to select design object and see how they are placed in the physical device. The Global Context pane allows you to see and zoom in the chip view when the view in the Physical Device pane is zoomed in tight. The Status Banner indicates whether the mode is Stroke mode or Select mode and how many instances are selected.

Figure 3-2. The Physical Window Layout



Understanding the Left Mouse Button Actions

ZOOM TO AREA	Left Click, Drag, release - draws bounding box to zoom in on
SELECT OBJECT	Left Click on Instance - selects and highlights a single instance
SELECT AREA	SHIFT, Left Click, Drag, and Release - selects all instances in the bounding box
UNSELECT OBJECT	SHIFT, Left Click on Instance - unselects only that instance

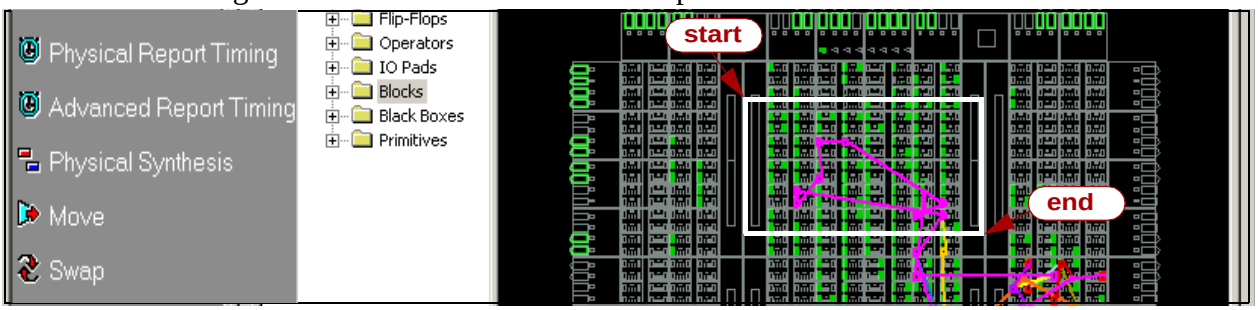
Changing the View with Strokes

You can right-click on the mouse to bring up the popup menu and accomplish many of the actions described in this section. However, many designers find that strokes are the fastest and most convenient method of transversing a view.

A stroke is an action where you press the Left Mouse Button, draw a line or bounding box, then release the button. The direction of the line indicates what action you want to take. For zooming strokes, the length of the line controls the amount of zoom. The strokes work in the Global Context view as well as the Physical Device View.

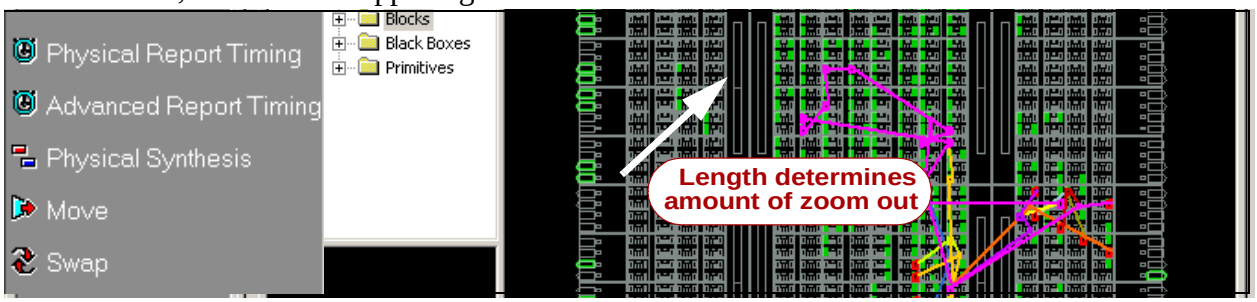
Zooming to Area

Draw a bounding box with the Left Mouse Button pressed.



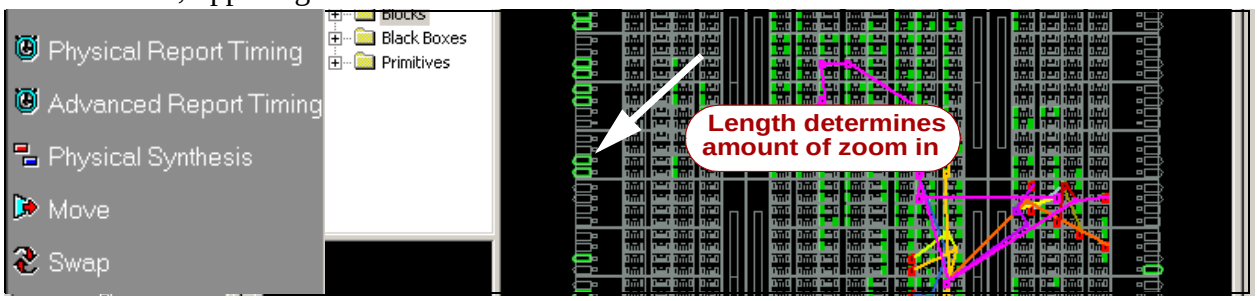
Zooming Out

Draw a line, lower left to upper right.



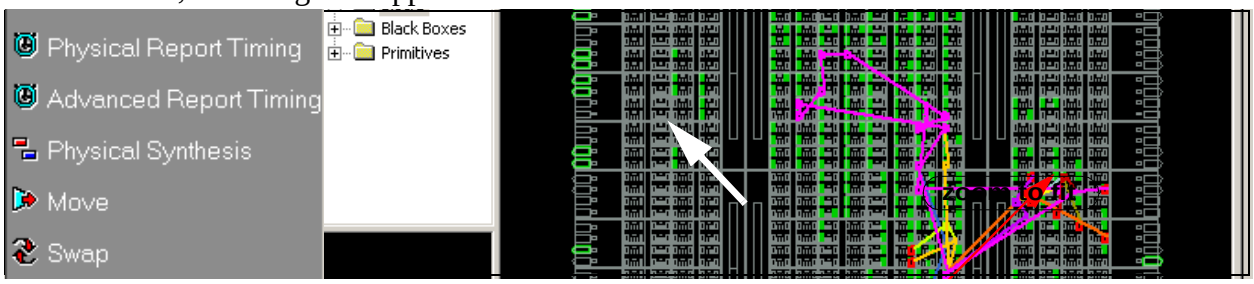
Zooming In

Draw a line, upper right to lower left.



Zooming to Fit

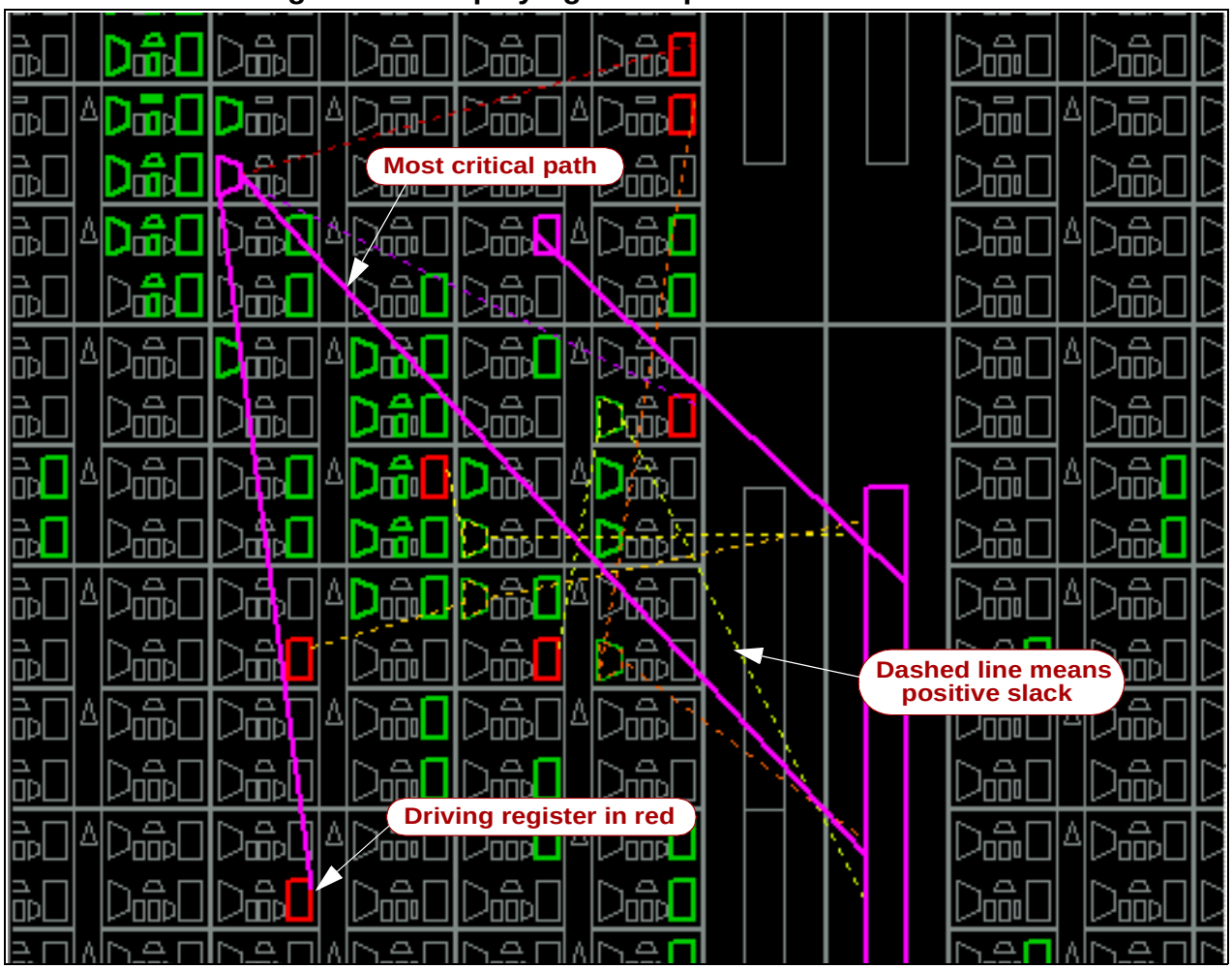
Draw a line, lower right to upper left



Displaying the Top Ten Timing Paths

You click the **Physical Report Timing** icon to generate a current timing report. And, as shown in Figure 3-3, the top 10 most critical timing paths are displayed with different colored lines between instances. Solid lines indicate negative slack. Dashed lines indicate positive slack. Driving registers are colored red. You can reduce the number of displayed paths and change color assignments with a right mouse clock, then select **Set Options > Physical >Display**.

Figure 3-3. Displaying the Top Ten Critical Paths



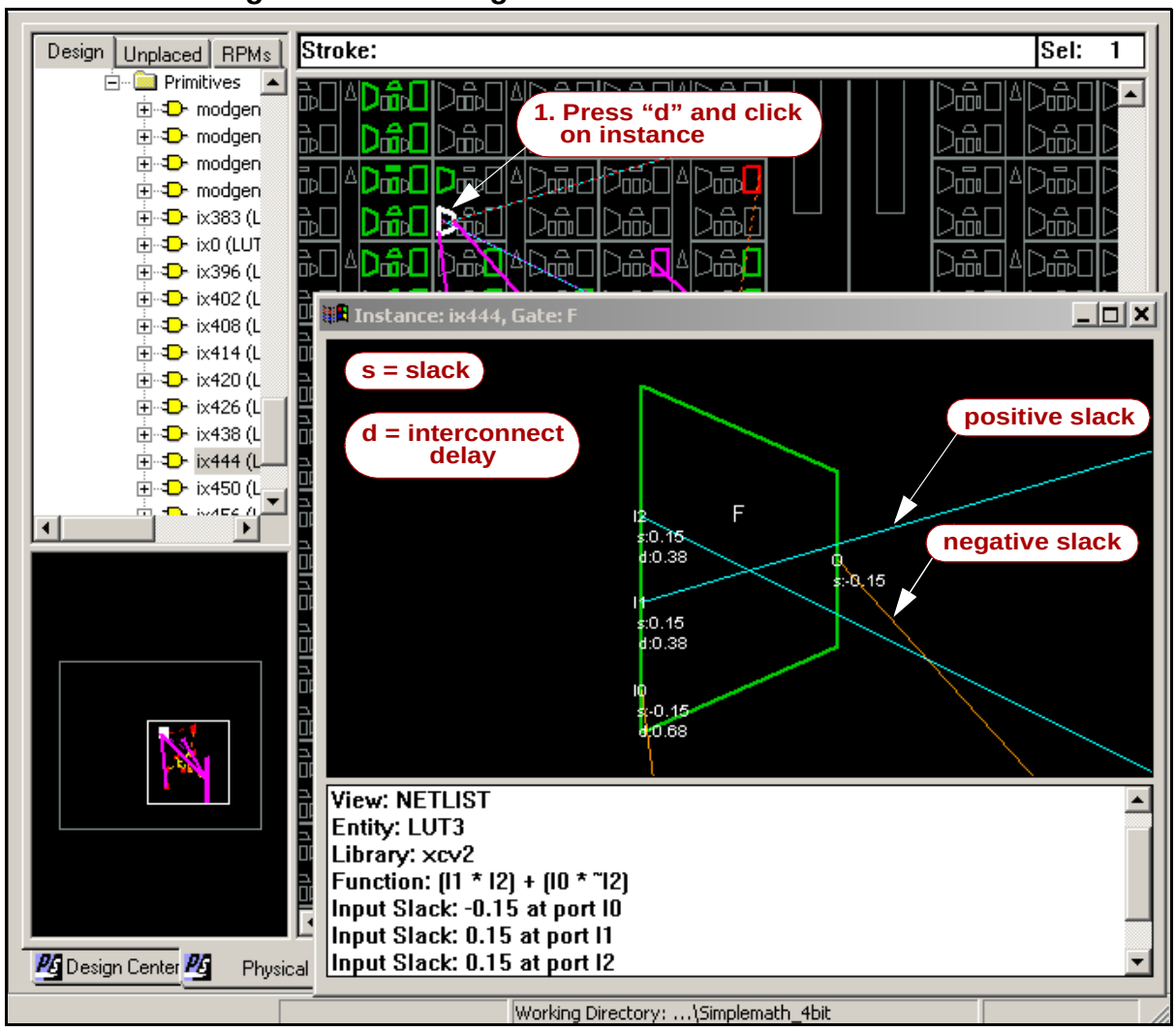
Creating a Detailed View of an Instance

To generate a detailed view of an instance, do the following:

1. Press the “d” key (for detail).
2. Click on an instance or slice.

In Figure 3-4, The detailed view of the LUT3 indicates one path with a positive .15ns slack and another with a -,15 negative slack. The interconnect delay of each route is indicated by the “d” value on each pin. The detailed view can be docked, and then takes the place of the global view.

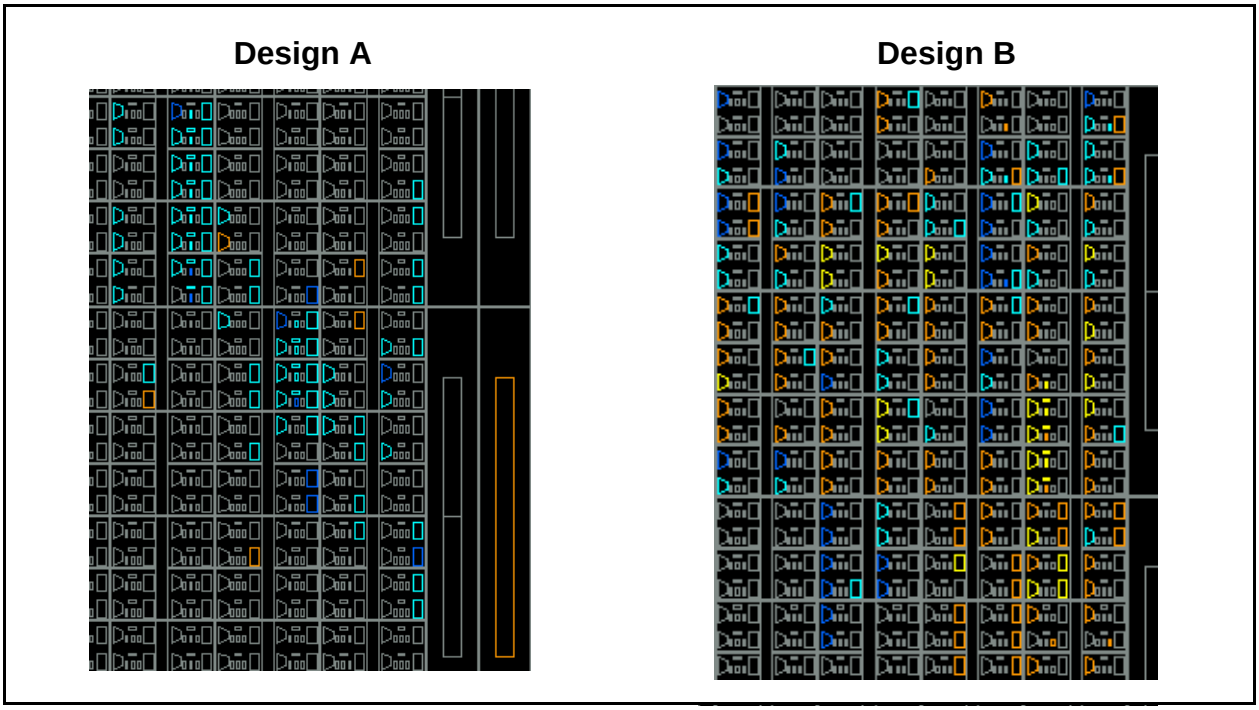
Figure 3-4. Creating a Detailed View of an Instance



Viewing Critical Instances

By default, the all instances are colored green. However, as shown in Figure 3-5, if you right-click and select **Display Critical Instances** from the popup menu, the instances are color coded to display where timing problems exist in the placement. If you turn off the display of timing paths it's easier to see. Notice that only a few instances in Design A are negative (orange). This design has a good chance of achieving timing closure. Design B, however, has a very dense pattern of orange and yellow instances. The chances of achieving timing closure in Design B are far less.

Figure 3-5. Viewing Critical Instances

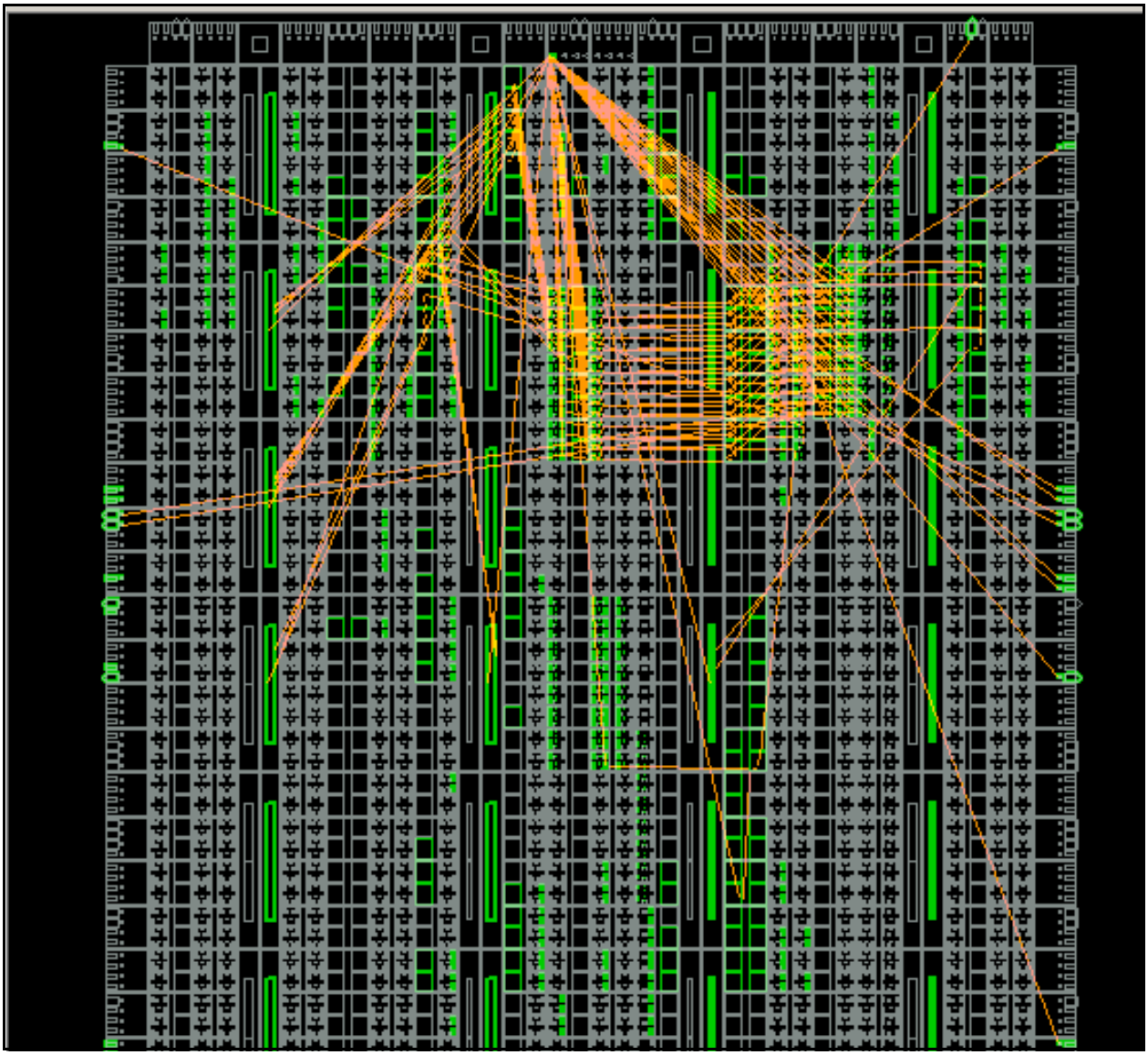


Viewing critical instances is excellent for finding areas of your fpga that are causing timing problems.

Viewing the Slack Graph

As shown in Figure 3-6, if you right-click, unselect Display Timing Paths, then select **Display Slack Graph** from the popup menu, all the interconnects with negative slack are displayed. The idea is to give you an overall view of the chip topography and where regions of critical placement exists.

Figure 3-6. Viewing the Slack Graph



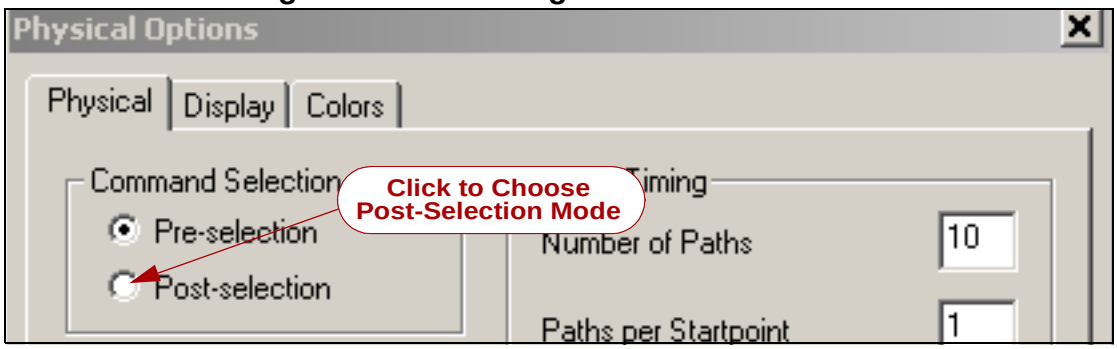
Setting Physical Options

You can quickly change the display options with a right mouse click. Select **Set Options...** > **Physical /Display/Colors**. The following provide further explanation of the display options.

Understanding Selection Modes

PreciseView can be in either Pre-selection mode or Post-selection mode. Pre-selection is the default mode.

Figure 3-7. Choosing the Selection Mode



Pre-selection Mode

In Pre-section mode, a command that requires selected objects can not be invoked unless objects are pre-selected. All commands that requires selected objects are greyed out until you select one or more objects.

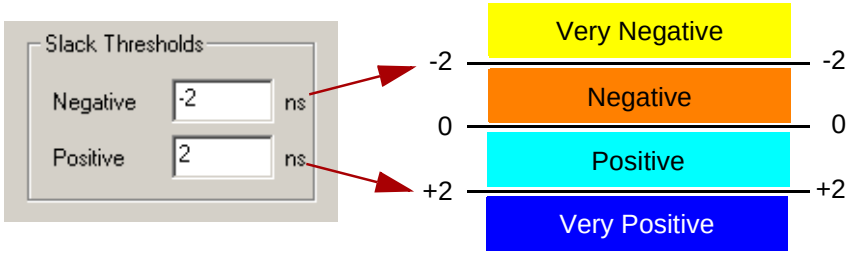
Post-selection Mode

If you choose post-selection mode as shown in Figure 3-7, a command that needs selected objects can be invoked even when there is nothing selected. The first thing the command does is prompt you to select one or more objects. If something is pre-selected, then the command uses this selection of objects.

Changing the Slack Thresholds

As shown in Figure 3-8, the **Negative Slack Threshold** defines the point where negative slack turns into very negative slack and the **Positive Slack Threshold** defines the point where positive slack turns into very positive slack. These Slack Thresholds can be changed with the **Set Options > Physical** Dialog box. The color of the regions can also be changed with the **Set Options > Color** dialog box.

Figure 3-8. Understanding Slack Thresholds



Changing the Critical Cover Threshold

The Critical Cover Threshold is a value that is used by the popup-menu function **Select Expand >Critical Cover**. When you select an instance then select this function, all instances that are connected to the selected instance that lie on a path with negative slack are selected. You might want to increase this value to a +1 or +2. This increases the number in selected instances on the perimeter of the cover and gives a function like **Improve Place > With Selected** more freedom to move instances without breaking other paths.

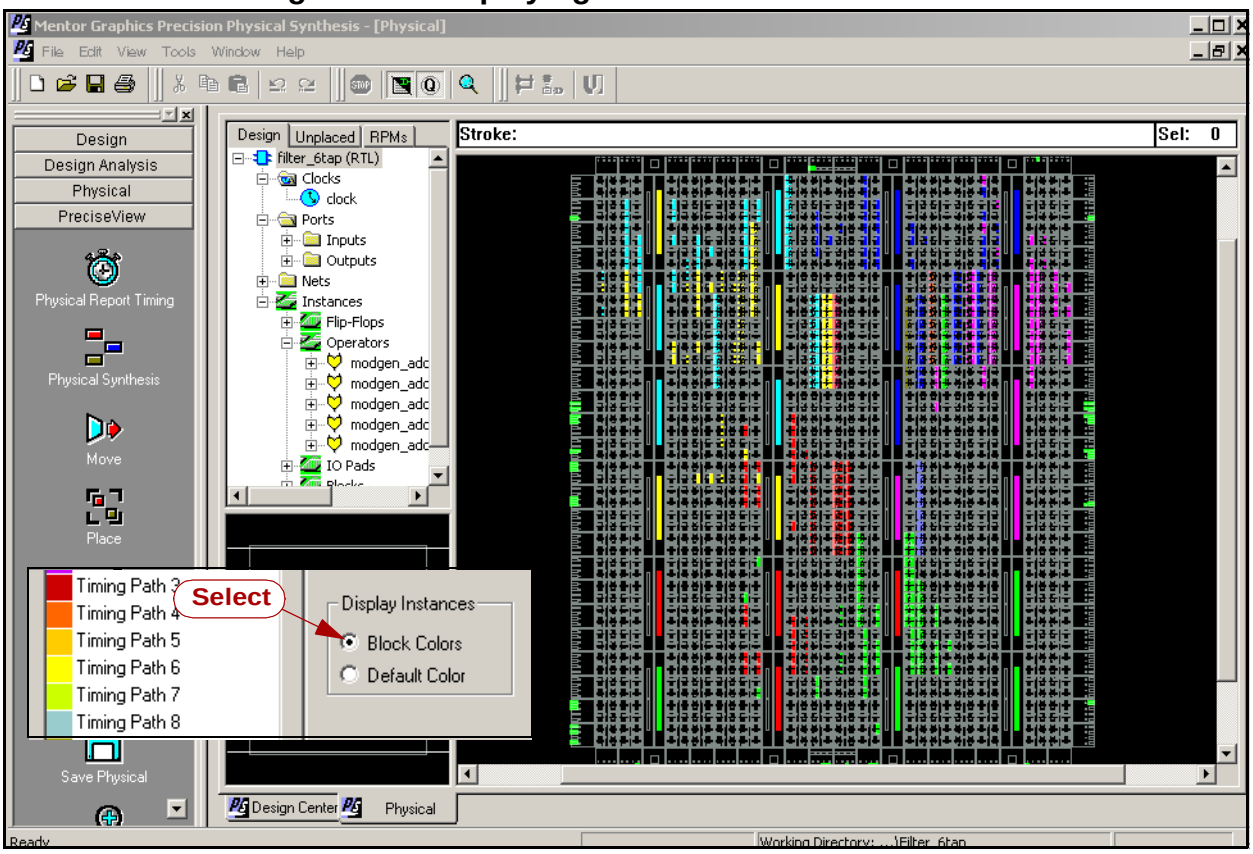
Changing the Level of Undo/Redo

There are 10 levels of Undo/Redo by default. This means that the last ten editing actions are saved in memory. If you are short on memory, you can reduce the number of Undo/Redo levels to improve the amount of available memory.

Displaying Blocks in Different Colors

If you have a hierarchical design, you can turn on the Block Colors display to see how the ISE tools placed the blocks. Figure 3-9 shows a filter design with six blocks. The **Block Colors** option has been selected from the popup menu **Set Options > Colors** dialog box as shown. Notice that some blocks are not tightly placed, but spread out. This can affect timing.

Figure 3-9. Displaying Blocks in Different Colors



Chapter 4
Interactive Fix-Up with PreciseView

Introduction

If your design does not achieve timing closure after running the automated physical synthesis flow, you may need to do some interactive fix-up. This Chapter describes a general methodology for approaching an interactive fix-up editing session.

Step 1: Invoke PreciseView 4-2
Step 2: Do a “Physical Report Timing” 4-3
Step 3: Select a Register/Start Point and Examine the Fanout and Slacks 4-4
Step 4: Use Select Expand > Critical Cover 4-5
Step 5: Use the “Improve Place” Algorithm 4-6
Step 6: Use Report Timing to See the Results 4-6
Step 7: Look for Instances that Can Be Moved to Shorten Interconnects 4-7
Step 8: Look for Registers that Can Be Replicated 4-8
Advanced Timing Report 4-9
- Moving an Instance 4-15
- Swapping an Instance with Another Instance 4-16
- Placing an Unplaced Instance 4-16

Step 1: Invoke PreciseView

Once Place and Route is completed, and the placement files are loaded, the PreciseView bottom pallet becomes available. Placement files are automatically loaded when Place and Route is run within the Precision tool. If Place and Route is run in the standalone vendor tool, it is necessary to load the data manually. These files include:

1. The Precision RTL-generated XDB file. (Or a synthesis-generated EDF and SDC file.)
2. The ISE-generated NCD file.
3. The pass ISE-generated DLY file.

The PreciseView button (ShowPicture) brings up PreciseView, which allows interactive editing of the physical implementation of your design.

Step 2: Do a “Physical Report Timing”

Scan the report to locate any big net delays as shown in Figure 4-1. For information on setting up your reports, see Advanced Timing Report.

Figure 4-1. Generating a Physical Timing Report

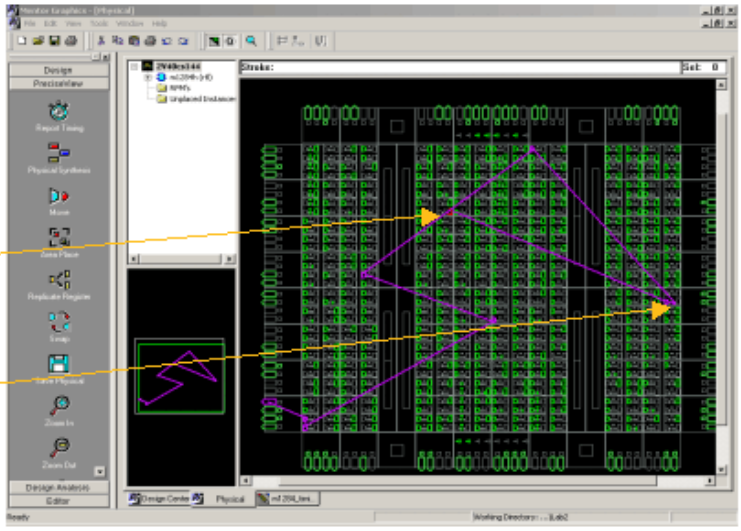
```
Critical path #2, (path slack = -1.46):

SOURCE CLOCK: name: vNIOW period: 24.000000
     Times are relative to the 1st rising edge
  DEST CLOCK: name: vCLK period: 12.000000
     Times are relative to the 2nd rising edge

NAME                              GATE      DELAY     ARRIVAL   DIR   FO
E1_reg_ECR_internal(5)/C          FDCE                0.00      up
E1_reg_ECR_internal(5)/Q          FDCE      0.43      0.43      up
ECR_dup0(5)                       (net)     2.01                      26
CONFIG/ix126/I2                   LUT4                2.44      up
CONFIG/ix126/O                    LUT4      0.33      2.77      up
```

Scan report for large (>0.5ns) net delays

This large net delay is clearly due to the distance between the register and the next LUT on the path.

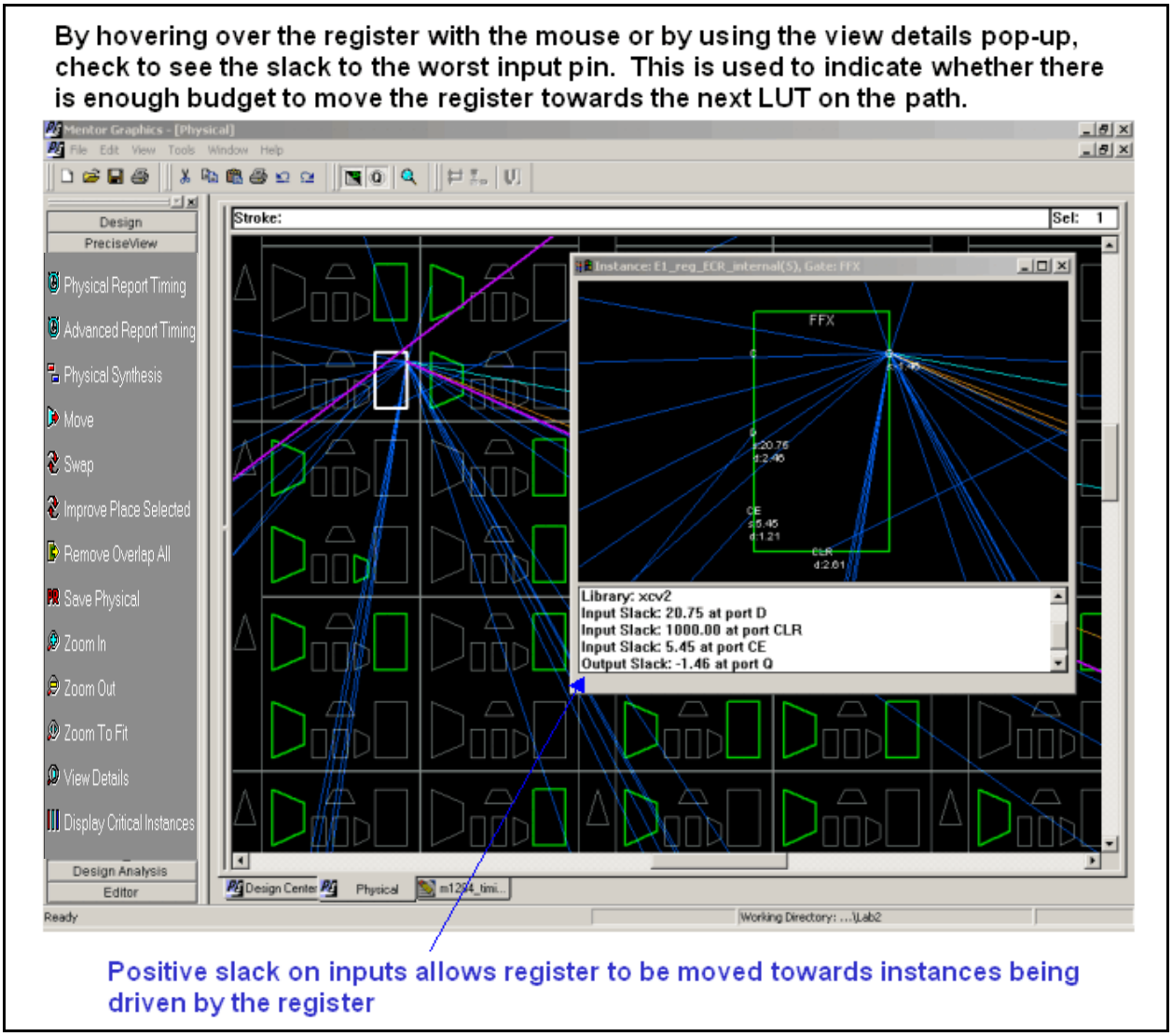
E1_reg_ECR_internal(5)

CONFIG/ix126



Step 3: Select a Register/Start Point and Examine the Fanout and Slacks

Figure 4-2. Select a Starting Point and Examine the Fanouts/Slacks


By hovering over the register with the mouse or by using the view details pop-up, check to see the slack to the worst input pin. This is used to indicate whether there is enough budget to move the register towards the next LUT on the path.
Mentor Graphics - [Physical]
File Edit View Tools Window Help
Design
PreciseView
Physical Report Timing
Advanced Report Timing
Physical Synthesis
Move
Swap
Improve Place Selected
Remove Overlap All
Save Physical
Zoom In
Zoom Out
Zoom To Fit
View Details
Display Critical Instances
Design Analysis
Editor
Stroke:
Sel: 1
FFX
Library: xcv2
Input Slack: 20.75 at port D
Input Slack: 1000.00 at port CLR
Input Slack: 5.45 at port CE
Output Slack: -1.46 at port Q
Design Center
Physical
Ready
Working Directory: ...\Lab2
Positive slack on inputs allows register to be moved towards instances being driven by the register

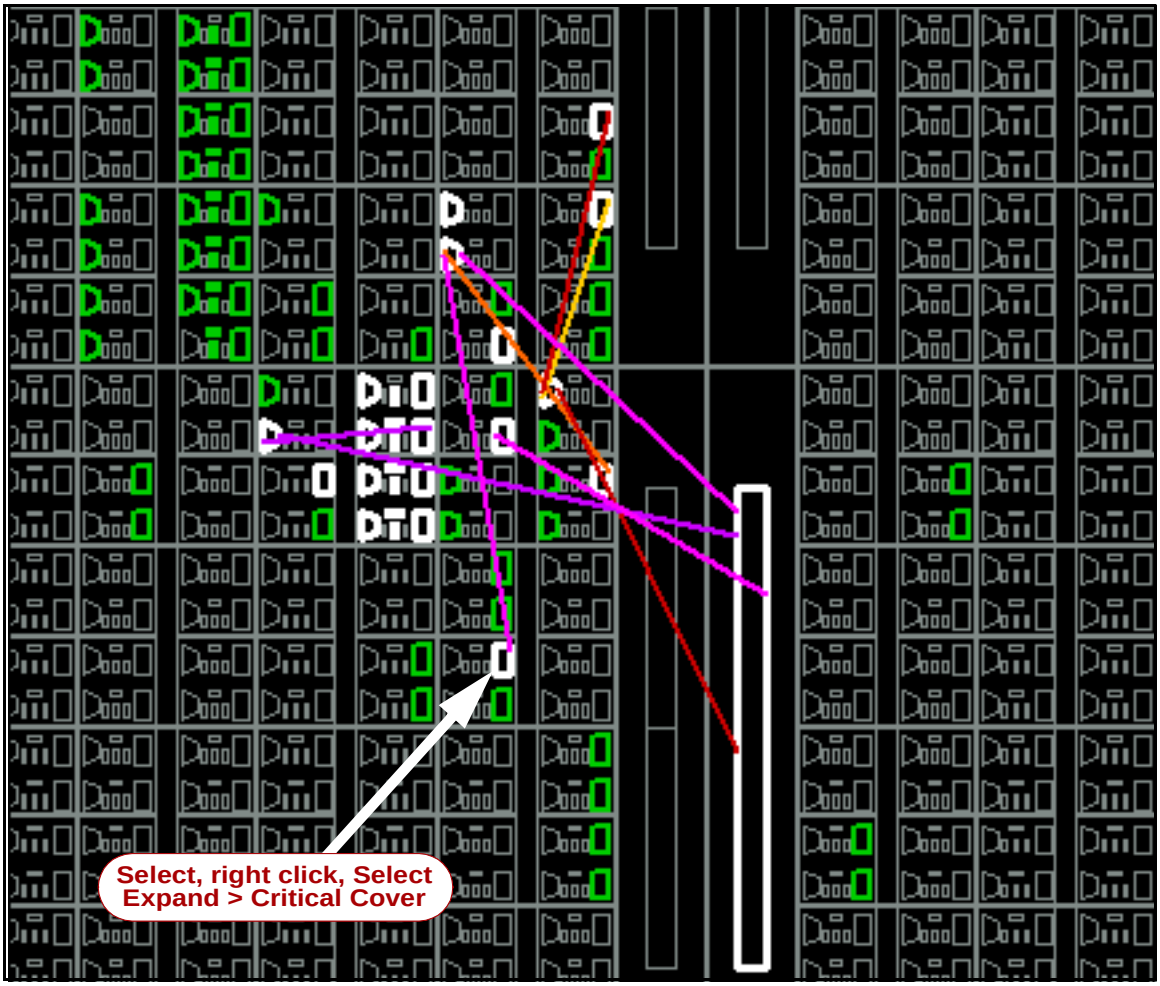
When an instance is selected, color coded flylines are drawn (in both editing and detailed view). These flylines help determine if an instance can be profitably moved, and in which direction. If there are critical routes (indicated by yellow or orange flylines) in all directions, moving that particular instance will not correct timing problems.

Step 4: Use Select Expand > Critical Cover

This is an important advanced selection function. When you select a instance on a critical path, this function does the following:

- PreciseView determines the start point and end point for the critical path that contains the instance. All instances connected to the specified critical path are selected if they are within the Critical Cover Threshold. By default, the Critical Cover Threshold is zero.
- However, if you change the threshold to +1 or +2, the number of positive slack instances selected on the perimeter will increase and the placement function has more freedom to move instances.

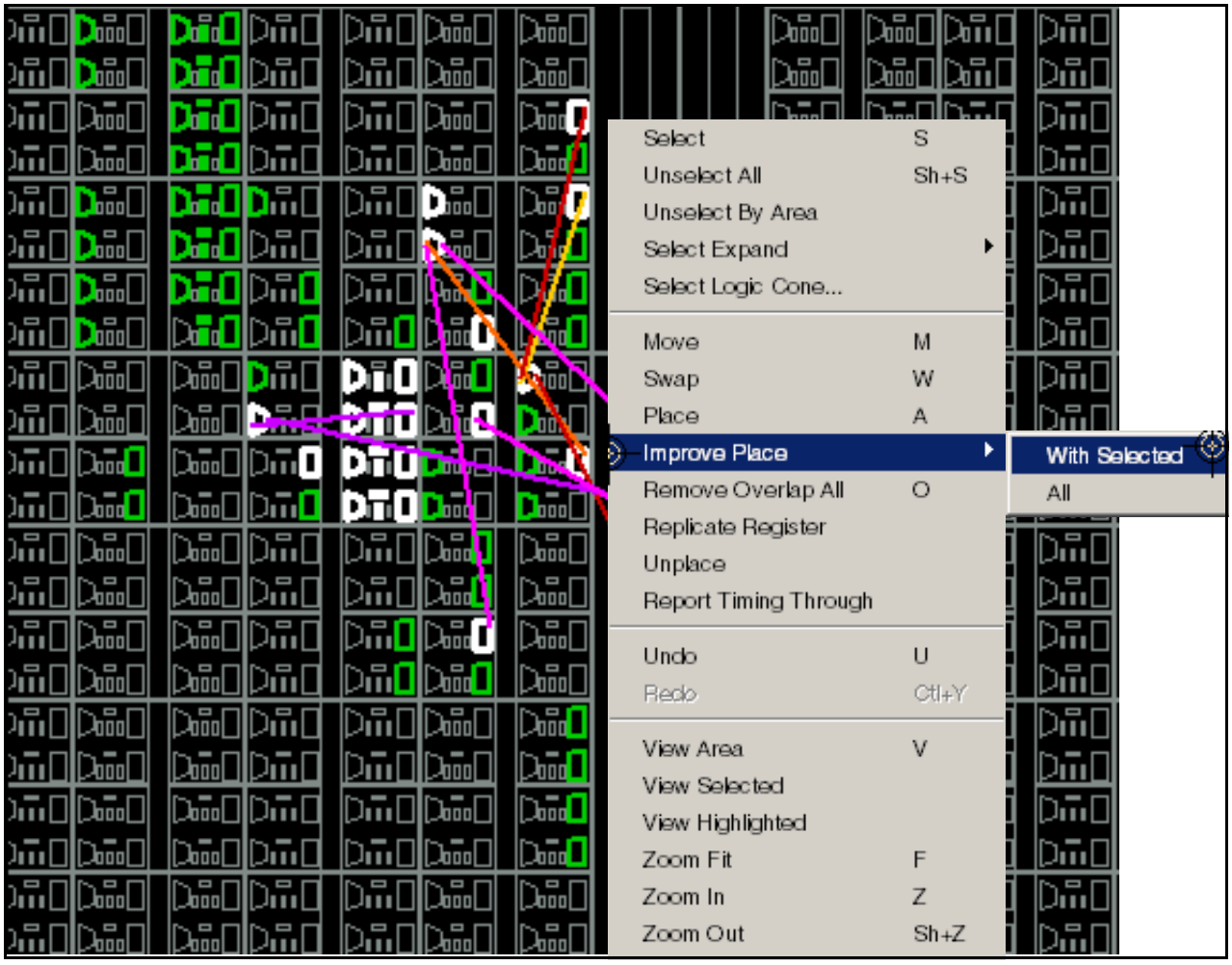
Figure 4-3. Using Select Expand > Critical Cover



Step 5: Use the “Improve Place” Algorithm

Right click and select **Improve Place > With Selected**. This algorithm uses maximum effort to improve the placement of selected instances.

Figure 4-4. Using “Improve Place With Selected”



Step 6: Use Report Timing to See the Results

Unlike the Physical Synthesis function, the Improve Place function does not execute an automatic Report Timing command. Click on the Physical Report Timing icon.

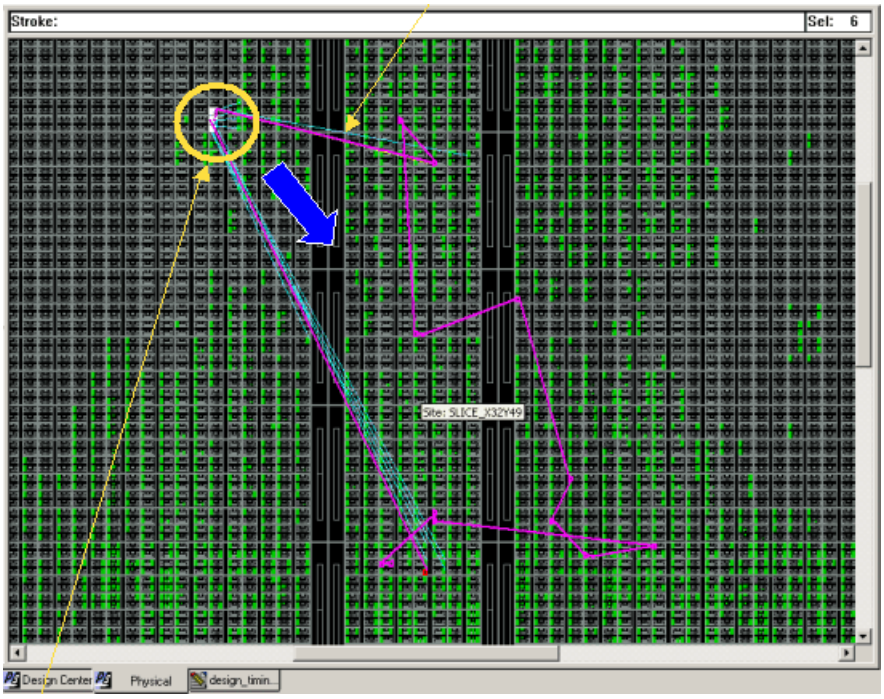
Step 7: Look for Instances that Can Be Moved to Shorten Interconnects

If the physical synthesis algorithms do not achieve timing closure, you can examine the layout and perform manual editing. Look for instances on reported critical paths that can be moved closer together.

Figure 4-5. Try to Shorten the Interconnects

Look for any adders and LUTs on the critical path that are contributing to a large delay. Try to move them towards the center of gravity. Often these can be clearly seen by looking at the highlighted critical path. Be sure to examine fanin and fanout so as to not break other paths.

Critical Path



Move badly placed cells towards center of gravity.

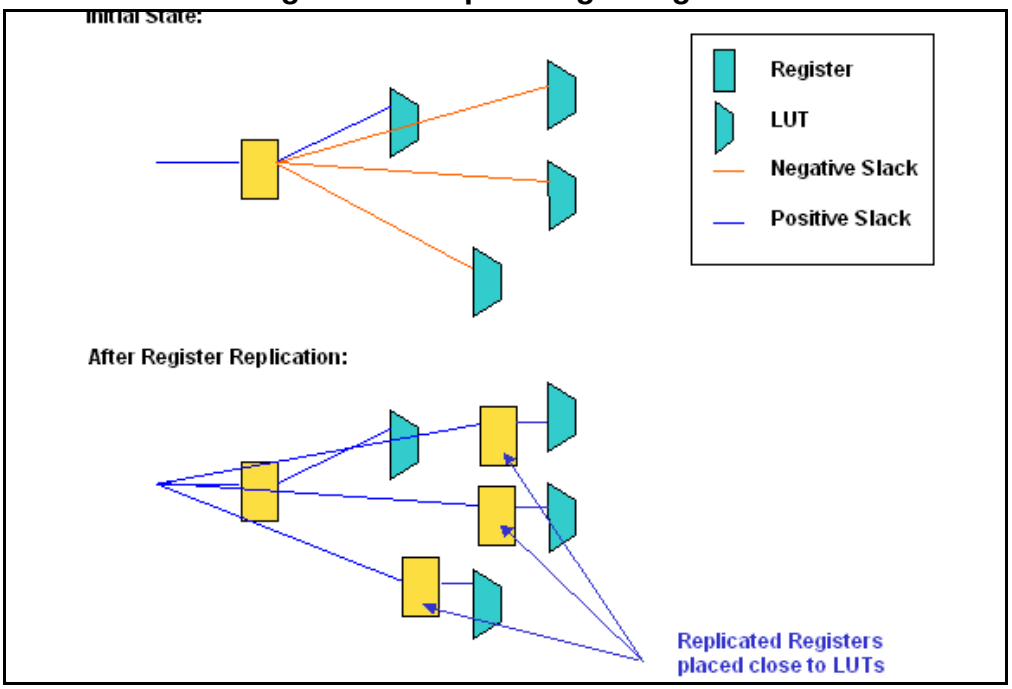
Step 8: Look for Registers that Can Be Replicated

If one fanout is critical, move the register towards the LUT on the path. If multiple fanouts are critical, it may not be possible to move the register towards the LUT without making other paths worse. In this case you should try register replication. Note that for register replication to be successful, there needs to be enough positive slack on the input side to allow the new register(s) to be moved closer to the LUTs directly connected to its/their outputs. Also, there must be negative output slack and multiple fanouts. This is represented in Figure 4-6.

The steps are as follows:

1. Select the register to replicate.
2. Choose “Replicate” from the popup menu. The tool will automatically add registers as appropriate.
3. Examine the replicated registers which will now be selected.

Figure 4-6. Replicating a Register



The Replicate register function can be undone, so if you are unhappy with the result, it is easy to back out. If ALL of the rules are not met, the command will fail and a message displays. Otherwise, the transcript will list the name of the new registers and all replicated registers will be selected, which makes it easy to see what changed.

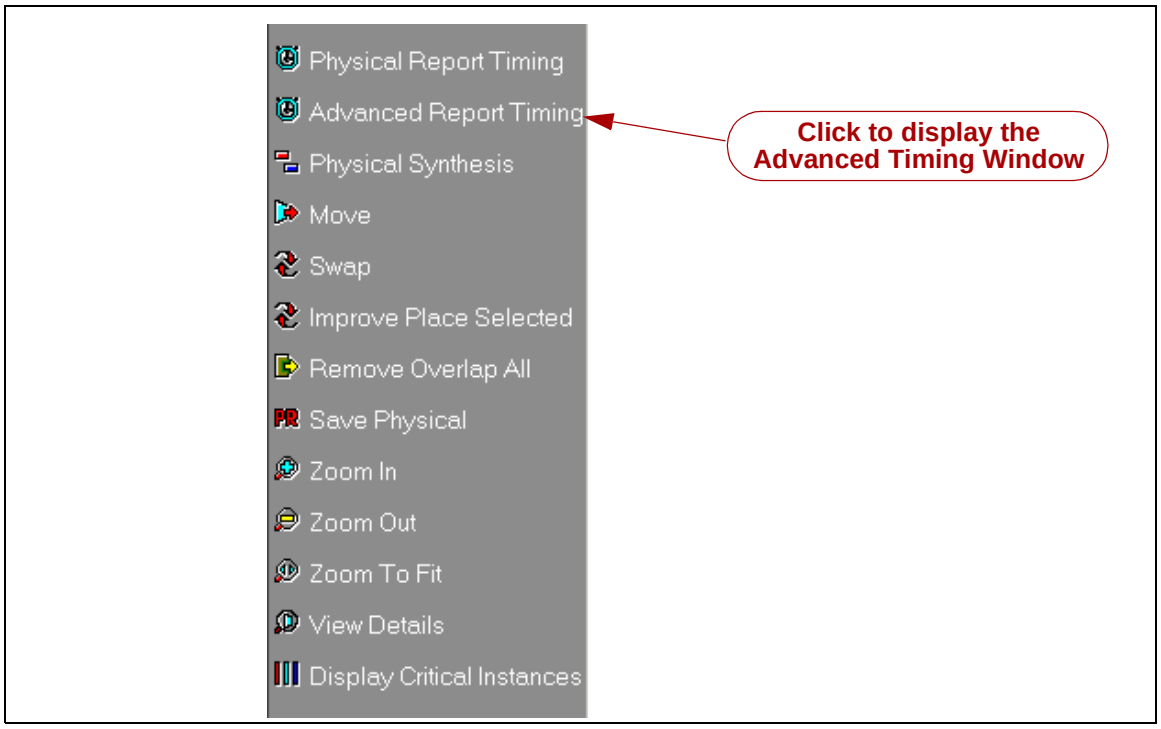
Advanced Timing Report

The Advanced Timing Report option lets you select portions of a design and then create timing reports for this specific area. Precision Physical lets you save data objects and settings from one report session to the next, allowing you to focus on a particular analysis as you improve the design until the desired results are achieved.

Setting Advanced Report Timing Options

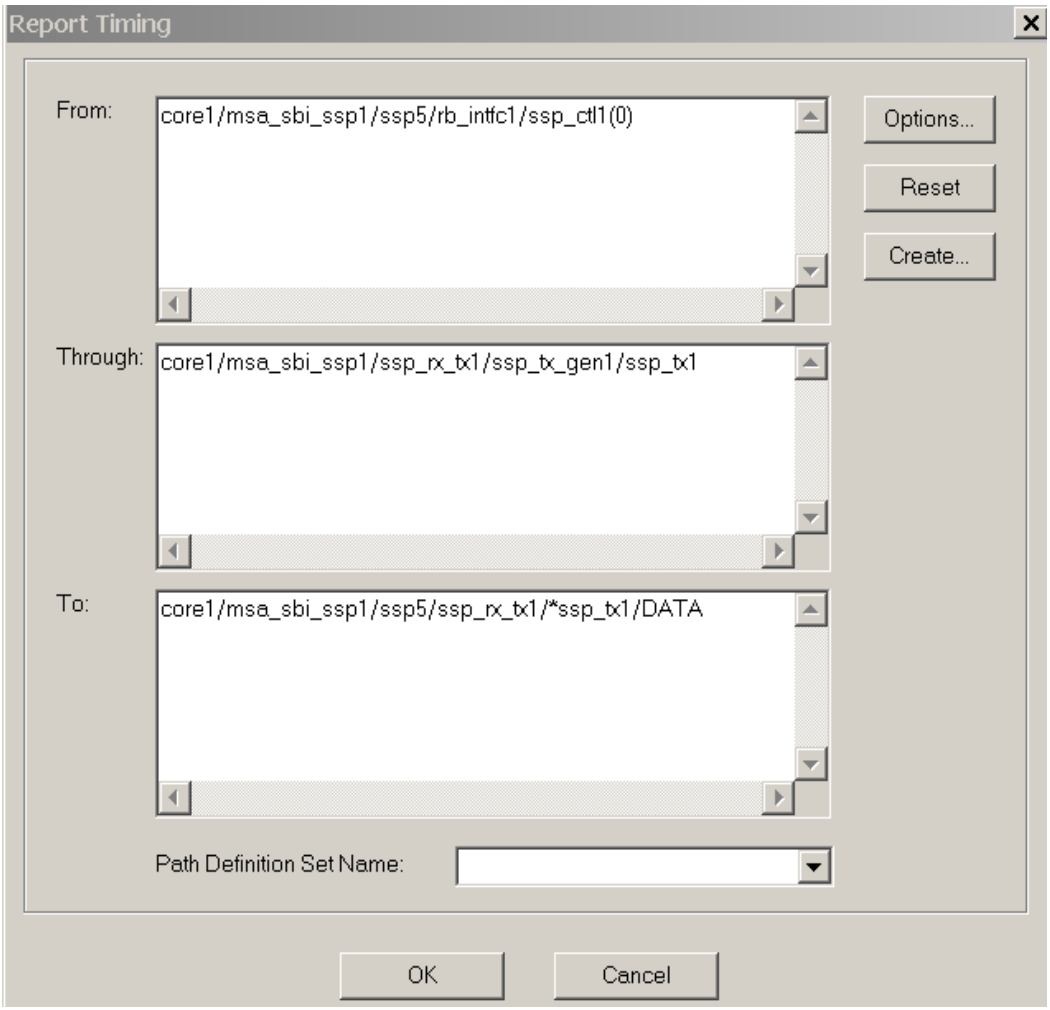
Use the Advanced Report Timing icon from the PreciseView tab to select report timing options:

Figure 4-7. Advanced Report Timing Icon



The Advanced Report Timing window displays.

Figure 4-8. Setting Advanced Report Timing



You can enter information in the From, To and Through fields using the following methods:

- Directly typing information in the From, Through, and To list areas.
- Building From, Through and To lists by selecting nodes from the hierarchical browser of Ports, Instances, Nets and Clocks and adding them to the appropriate list.
- Choosing information from a previously defined Path Definition set.

You can select an existing Path Definition Set from the drop-down list.

Click the **Reset** button to clear the From, Through, To and Path Definition Set Name fields.

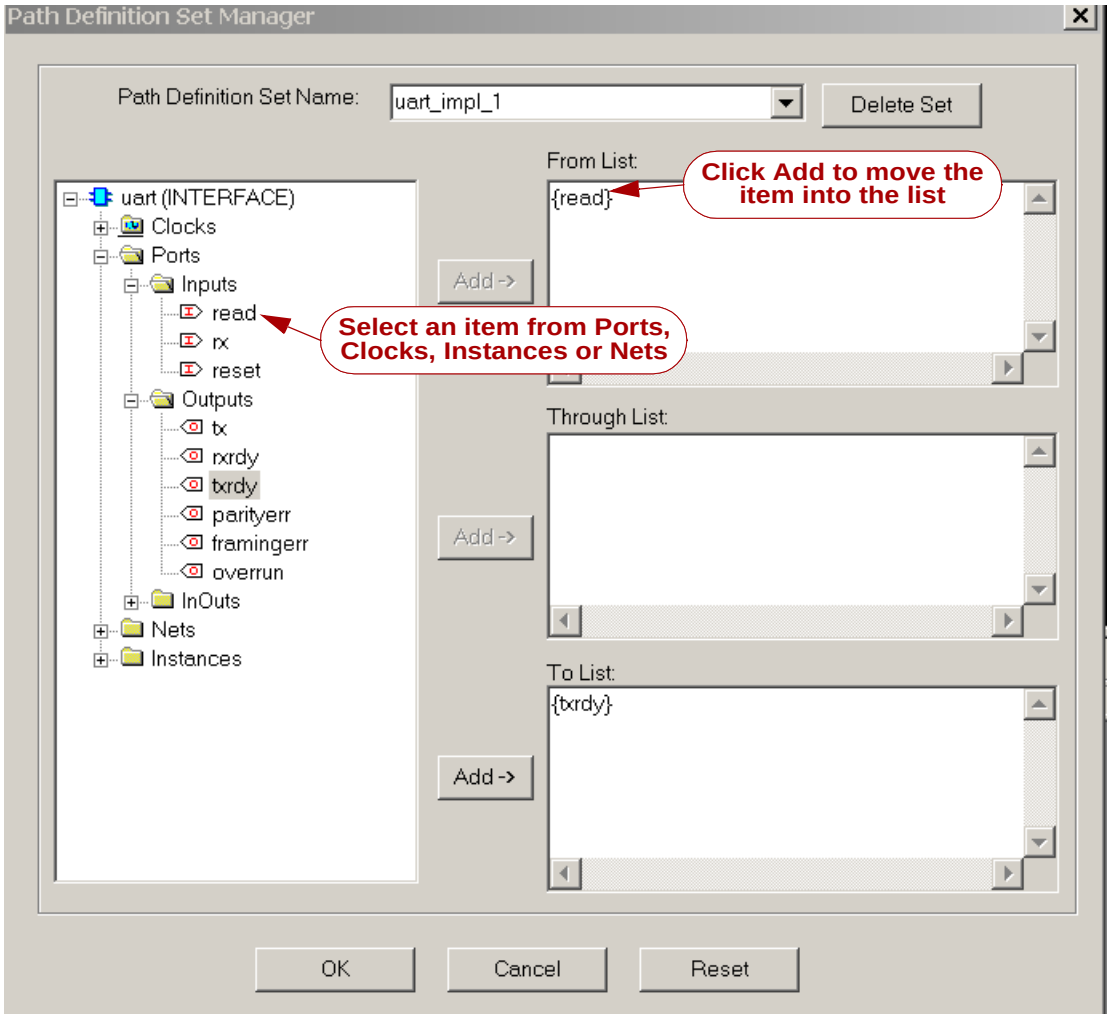
Path Definition Sets

The tool lets you specify from / through / to Path Definition sets to narrow the desired timing paths to be analyzed. You can save a Path Definition to an external file and then re-load these Path Definition sets to help with the re-evaluation of specific timing concerns after design iteration. The Path Definition sets are automatically saved into an external file during the Save Project operation and are restored during the Open Project operation so that they are available for access throughout Precision. The tool also allows you to set command options affecting the contents and the look of the timing report.

Creating Path Definition Sets

The following section describes how to create a Path Definition Set and select items for the From, Through and To list areas. Click on the Create button to display the Create window.

Figure 4-9. Create a Path Definition Set



Path Definition Set Name

Type the name for the Path Definition Set name or select it from the drop-down list.

From / Through / To Lists

Select the design element that you want to include in a list from the Clocks, Ports, Nets, or Instances. Click one of the **Add** buttons and the element is added to the list. Depending on the object selected, some "add" options might be inappropriate and the Add button will be grayed out (not accessible). Continue this process until all of the design elements you want in your timing report are added.

Click **Reset** to clear the fields.

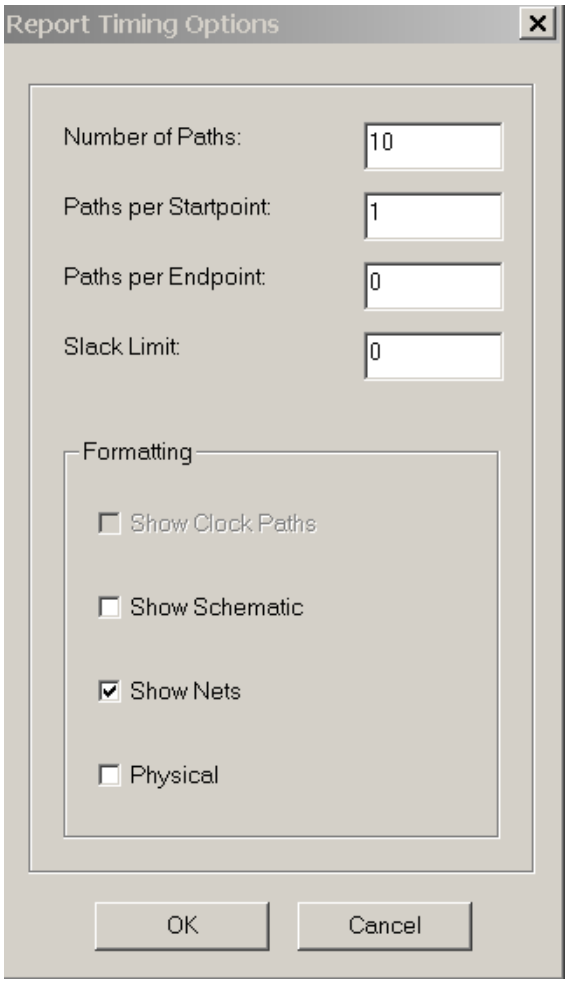
Click **OK** and the tool saves the Path Definition Set as a TCL file. Existing Path Definition Sets can be loaded or revised in Precision Physical.

Set Report Timing Options

Use the Report Timing Options dialog box to set specific options for your timing report. Select this dialog by clicking the **Options…** button on the Report Timing dialog. The very first time this dialog is opened in the session, its fields are populated with the values of the same options of the Physical Options page. An example of this dialog box is shown in Figure 4-10.

The Physical Options page can be brought up either through **Tools | Set Options | Physical** or through the **Set Options…** menu item of the PreciseView pop-up menu.

Figure 4-10. Set Report Timing Options



Type a desired numeric value in the Number of Paths, Paths per Startpoint, Paths per Endpoint, or Slack Limit.

Note: Using Paths per Startpoint is much more efficient than using Paths per Endpoint. Specifying “0” for these options disables the operation of the option.

Formatting

Check the box to indicate if you want to show the Schematic, Nets or Physical on the timing report.

Click **OK** to accept the settings.

Displaying a Timing Report

Click the Physical Report Timing icon on the PreciseView Pane or enter the `report_timing` command in the Transcript window to display a timing report. An excerpt from a timing report is shown below.

Figure 4-11. Timing Report

```
# -- CTE report timing..
# Physical wire delay calculation is used in this process ...
#                   CTE Critical Path Report
# -- CTE get true worst setup path..
#
#
# Critical path #1, (path slack = 10.76):
#
# SOURCE CLOCK: name: write period: 20.000000
#      Times are relative to the 1st rising edge
#   DEST CLOCK: name: write period: 20.000000
#      Times are relative to the 1st falling edge
#
# NAME                GATE                    DELAY    ARRIVAL DIR
# data(6)           (port)                                0.00   dn
# data_bdbuf(6)/IO IOBUF(LVTTL,SLOW,12)                   0.00   dn
# data_bdbuf(6)/O  IOBUF(LVTTL,SLOW,12)        0.67       0.67   dn
# lat_txhold(6)/D  LD                                     0.67   dn
#
#     Initial edge separation:      10.00
#     Source clock delay:      -     0.00
#     Dest clock delay:        +     1.72
#                              -----------
#     Edge separation:              11.72
#     Setup constraint:        -     0.29
#                              -----------
#     Data required time:           11.43
#     Data arrival time:       -     0.67
#                              -----------
#     Slack:                        10.76
```

Using Keyboard Shortcuts for Simple Edits

The Shortcuts

You can right-click on the mouse to bring up a popup menu to accomplish many of the actions described in this section. However, many designers find that a combination of left-mouse clicks (to select instances) and pressing a key (a keyboard shortcut) the most efficient method to execute editing commands. The following list summarizes the available keyboard shortcuts.

```
report timing  "Shift+T"
place          "a"
swap           "w"
remove overlap "o"
view details   "d"
view area      "v"
zoom fit       "f"
zoom in        "z"
zoom out       "Shift+Z"
move           "m"
redo           "ctl+Y"
select         "s"
unselect all   "Shift+S"
undo           "u"
cancel         "esc"
```

Moving an Instance

Note

The Keyboard Shortcuts do not currently work properly on Sun Solaris.

1. Click on an Instance or instance group (like a carry chain). Object turns white
2. Press the “m” key (for move)
3. Click an un-occupied area (of like kind) in the template
4. If a yellow box appears, press “o” to remove the overlap
5. Press “Shift s” to unselect the selected object(s)
6. Press “Shift t” to report the new timing

7. Press “u” to Undo if you don’t like the placement

Swapping an Instance with Another Instance

You can use the following procedure to swap a critical instance with a non-critical instance.

1. Click on an Instance (like a critical-path register). Object turns white.
2. Press the “w” key (for swap)
3. Click on a non-critical-path register
4. Press “Shift s” to unselect the selected object
5. Press “t” to report the new timing
6. Press “u” to Undo if you don’t like the placement

Placing an Unplaced Instance

You can use the following procedure to place an un-placed instance.

1. Click on the Unplace tab in the Browser pane.
2. Click on an unplaced instance, then right-click and select “Place”.
3. Move the curser to the Physical Device pane and click on an un-occupied area.
4. If a yellow box appears, press “o” to remove the overlap
5. Press “Shift s” to unselect the selected object.
6. Press “u” to Undo if you don’t like the placement or “m” to move the instance.

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